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Subject:	**PCD2.M150**	**FW VERSION**	**V0F1**
Doc #:	**PCD2M150_0F1_Overview.doc**		

PCD2.M150 SUMMARY OF FIRMWARE VERSIONS

This document summarizes the changes of all firmware versions that are liberated on the PCD2M150 for production.

Concerning corrected / known bugs:
Only important bugs are listed here. For other bugs, please refer to the file COMSWER.XLS that contains more information about known bugs.

FEATURES OR RESTRICTIONS SPECIFIC TO PCD2.M150

General

- FW update (starting from version 0D0):
  The FW can be updated with the FW downloader. To start this program click "PCD FW downloader" in the "tools" menu from the PG5 Saia Project Manager.
  The FW update can only be done through the PGU port (port 0).
  A FW update is possible with the AMIC FLASH A29040 but not on the ATMEL FLASH 49F040.
- CPLD programming:
  At first power up after a firmware update note that the CPLD will be reprogrammed if its version is different.
  Please do not interrupt this programming sequence which take about 30 seconds, but in some case it can take until 2 min. (LED's are all off while programming, and blinking in the normal boot sequence when finished).

  FW Version history ↔ CPLD Version

FW Version	..., $94	0A0, 0B0, 0B2, 0B6, 0B7, 0C0, …
CPLD Version	MF26	mF28

- PGU
  Default PGU mode is S-BUS parity therefore PG5, PG4 from version V1.3 upward or PG3 from version β2.0 upwards have to be used.

Memory

- User memory:

User program memory	HW	System Memory	Default Memory configuration
None		128 / 0 kByte	24k prg lines, 32k txt/db
RAM / EPROM			
	1 Mbits	128 / 128 kByte	24k prg lines, 32k txt/db, 128k extended txt/db
	4 Mbits	512 / 128 kByte	96k prg lines, 128k txt/d, 128k extended txt/db
FLASH			
	1 Mbits	112 / 128 kByte	21k prg lines, 28k txt/db, 128k extended txt/db
	4 Mbits	448 / 128 kByte	84k prg lines, 112k txt, 128k extended txt/db

Note:
- At first memory configuration the FW makes an allocation with the maximum space available depending on the RAM/EPROM/FLASH chip.
- Extended txt/db (txd/db number >= 4000) use fast indexed access and support binary zero insertion, lower range txt/db have a slower access and do not support binary zero insertion.
- There is no extended txt/db if no optional memory chip is added.
- With EPROM and FLASH as user program memory the txt/db < 4000 are read only. With RAM the txt/db < 4000 can be set to read only using the WP on board jumper.
- The setting of bindings in LON (LON commissions) is only possible if RAM is used and the read protection jumper is not set.

- EEPROM:
  - The S-Bus configuration is automatically saved in the EEPROM, this means that even if the battery becomes discharged the S-Bus configuration will be safe.
  - There are 50 non-volatile user registers.

Instructions

- NOP
- Instruction set to ~5µs for FB's compatibility V0A0

- LD=/LDX=
- FB's parameters can be use on the LD and LDX instructions. V0D0

- SASI
- Text accepts $R parameters. V0A0
  E.g:"UART:$Ra,$Rb,$Rc,$Rd;MODE:$Re,$Rf;DIAG:FRg,RRh;"

a	Baudrate	110…38400 (numerical value)
b	Bits	7,8 (numerical value)
c	Parity	E,O,N (ASCII coded)
d	Stop	1 or 2 (numerical value)
e	Mode	'MC0', 'SM2', etc. (ASCII coded)
f	Station	Reg. with S-Bus station (numerical value)
g	Diagnostic flags	Reg. with the base diag. flag nbr (0..8191 num. value)
h	Diagnostic register	Reg. with the diag. register nbr (0..4095 num. value)

- SYSRD/SYSWR
- SYSRD/SYSWR/SYSCMP/DEFTR instructions. V0A0
- SYSWR 1000: System watchdog V0B0
- SYSRD 660x for serial port mode read back added V0D0
- SYSRD/SYSWR 7050 to 7081 V0A0
  to read and write the different elements of the clock.
- SYSRD 7090 V0A0
  Function that returns the number of seconds elapsed since 00:00:00; January 1; 1970 (coordinated universal time), according to the system clock.

- SF
- IP library V0A0
  Added SF "ReadIPConfig" V0E0
- Application library V0D0
  including SFs "CopyText", "InitDB", "CopyDB2Registers", "CopyRegisters"
  New "CopyBytes" SF V0F0

Communication

- Serial communication:
  - MC0/1/2/4, MD/SD, MM4 V0A0
  - MC5 mode that deactivate RS-485 drivers directly after completion of transmission. V0C0
  - Freeze function for the MC mode to ensure that no inter-character delay take place during the transmission of a frame. V0F0
- S-Bus:
  - Parity and break modes as master and slave. V0A0
  - Data-Mode V0A0
  - Secure Data Mode V0E0
    Option to disable the S-Bus secure data mode V0F0
  - Modem+ V0A0

- Gateway (GM/GS). V0A0
- New S-Bus configuration data handling (Station no., config. S-BUS) when inserting a programmed user memory (EPROM/FLASH). V0A0

- S-RIO as master and slave. V005
  The S-RIO master task assumes the communication and the refresh of the process image. The RIO task is activated by a SASI instruction. The SAIA configurator automatically generates the SASI text, the configuration and messages DB. For more information please read the document “Remote I/O with SAIA S-Bus” 26/751 F2.
- PROFIBUS FMS with PCD7.F700:
  - Base functionality V0A0
    10 channels (10...19) and 100 objects (100...199).
  - Extension (at least SPROF $137 is needed) V0A0
    possibility to map objects on DBs, read/write indicator, multicast/broadcast link, watchdog.
  - Extension for profile GA V0A0
- PROFIBUS DP: V007
  - Master mode with PCD7.F750.
  - Slave mode with PCD7.F77x.
  - Introduced signed values V0B0
- LON with PCD7.F80x:
  - Base functionality V0A0
  - LON enhancement with new functionality poll and alias (LON 1.5). V0C0
- Communication on TCP_IP with PCD7.F650/F652:
  - S-Bus over UDP/IP V0C0
  - “Open data mode” over TCP or UDP V0C0
  - SMTP E-Mail support V0D0
  - DHCP / UDP with the PCD7.F655 V0D0
- Web server V0D0
  - S-Web Alarming V0B0
- DHCP / UDP with the PCD7.F655 V0D0
- PGU switches automatically to 38.4 kBds (requires PG5 V1.2). V0C0
- Up to 2 ports could be configured/assigned at 38.4 kBds at the same time. V0C0
- It is possible to configure/assign port 0 (or 1) at 38.4 kBds and port 1 (or 0) at19.2 kBds. V0C0

Miscellaneous

- New features for PG5. V0B0
  - New OUTL and OUTLX instructions
  - New synchronization for a bloc downloads in mode “RUN”
  - Possibility to upload data (SEDIT and SFUP) in a synchronized manner.
- XOB
  - XOB 20, 25: interrupt inputs XOB's V0A0
  - XOB 17, 18, 19: User XOB's V0A0

This XOB's which can be provoked via S-BUS telegram (STXM chan, 0, k 4000, k 17..19) or SYSWR command (K4017..K4018). The XOB's are only executed if the CPU is in RUN or CONDITIONAL RUN.

- XOB 7: System overload XOB V0A0
- XOB 14/15: Cyclic XOB's
  can be executed from 5 ms to 1000s with 1ms steps V0A0
- New XOB handling. V0A0
  During the execution of a XOB other XOBs are queued and executed at the end of the first one.

- Calculation of week and day number V007
  The PCD compute the day and the week number based on the date using the same algorithm as in the PG. The command 'Write Clock' corrects automatically the week number or day number if they are wrong.
- Password mechanism. V003