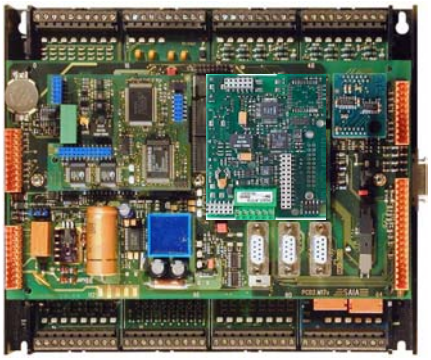
Contents

Simatic®, STEP® , Siemens® , S7-300® and S7-400®

are registered trademarks of Siemens AG

7.3 PCD2.M177 controller

7.3.1 PCD2.M177, performance characteristics



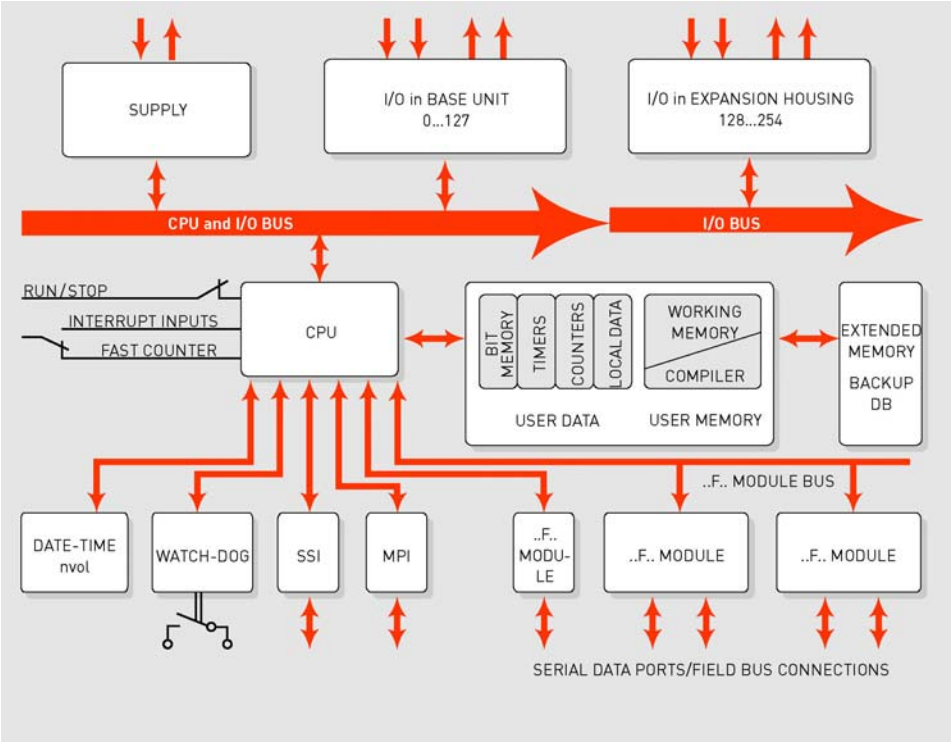
The PCD2.M177 base unit consists of:

- a lower part with I/O bus and main printed circuit board
- a snap-on cover, on which the operational controls are labelled

Eight I/O modules can be plugged onto the I/O bus (four each, along both sides).
With an expansion housing, up to 16 module spaces are available.
The user has a free choice of module space.

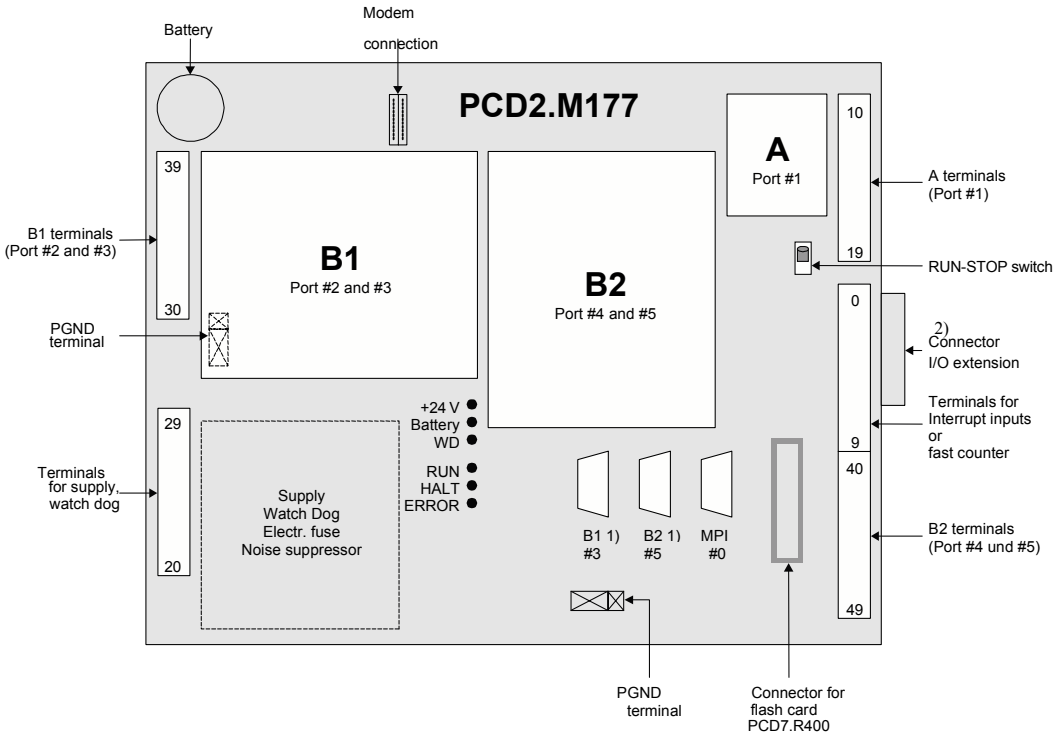
Function	**PCD2.M177**
Firmware	on SMD - Flash
I/O and modem modules	All PCD2 modules can be used
Expansion housings	PCD2.C107 PCD2.C157 PCD4.C225
MPI	RS485
Serial port # 1	Socket A
Serial port # 2 & 3	Socket B1
Serial port # 4 & 5	Socket B2
Network modules	Socket B1 / B2
Processor	68340 @ 25 MHz
Speed	~1ms for 1000 instructions (Command mix)
User memory: - RAM, battery buffered - Memory module	 Settable up to 1024 KByte PCD7.R400 (1024 KByte Flash Memory)
Programming tool:	Step®7-Mini from Siemens® Step®7-Light from Siemens® Step®7 from Siemens® Step®7 Programming tool from third supplier

7.3.2 PCD2.M170 block diagram



7.3.3 Pin configuration and operational controls

The illustration shows the main board of the PCD2.M177 (with maximum equipment).



1) The pin configuration of these two D-Sub connectors (9 pole female) complies with the PROFIBUS standard. The two D-type connectors should preferably be used for PROFIBUS networks. All other serial ports should, if possible, be connected to the 10-pole plug in screw terminals.
2) I/O extension: For this connection there are special ready-made cables

With its cover removed, the PCD2 shows all active components apart from the I/O bus printed circuit board. This is located below the main board on a level with the I/O modules.

Caution:
Removal of the cover exposes components that are sensitive to electrostatic discharges.
When the supply is connected, no manipulations should be carried out (such as changing jumper positions or inserting/removing I/O modules, etc.).
Batteries can be changed while the supply is connected, without loss of data and in all operating modes. This procedure does not necessitate removal of the cover.

Pin configuration, ports #0 to #5

Interrupt and/or counter, SSI interface		Serial data ports, socket A Port #1						Supply Watch-dog	
Terminal 0...9		Terminal 10...19	RS 485 PCD7.F110	RS 422 PCD7.F110	RS 232 PCD7.F120	TTY/20 mA PCD7.F130	RS 485 galv. PCD7.F150	Terminal 20...29	
0	SSI Data in +	10	PGND	PGND	PGND	–	–	20	+24V
1	SSI Data in –	11	RX – TX	TX	TXD	TS	RX – TX	21	+24V
2	IN A2	12	/RX – /TX	/TX	RXD	RS	/RX – /TX	22	+24V
3	IN B2	13	–	RX	RTS	TA	–	23	PGND
4	SSI Clock out +	14	–	/RX	CTS	RA	–	24	PGND
5	SSI Clock out –	15	–	PGND	PGND	–	–	25	WD
6	+	16	–	RTS	DTR	TC	–	26	WD
7	OUT 2	17	–	/RTS	DSR	RC	–	27	–
8	PGND	18	–	CTS	RSV	TG	SGND	28	–
9	PGND	19	–	/CTS	DCD	RG	–	29	–

Serial data ports sockets B(1) and B2: screw terminal blocks/ 9 pole D-type									
Port #	Terminal B(1)	Terminal B2	RS232 + RS485 PCD2.F520/..F530	RS485, PCD7. ..F722/..F802	RS232 + RS422 PCD2.F520/..F530	2xRS232 PCD522	RS232 full PCD2.522	MPI / RS485 Port #0	
Port #2/4	30	40	PGND	PGND	PGND	PGND	PGND	Sub-D	
	31	41	TXD	RX - TX	TXD	TXD	TXD	1	—
	32	42	RXD	/RX - /TX	RXD	RXD	RXD	2	M24V
	33	43	RTS	—	RTS	RTS	RTS	3	LTG_B
	34	44	CTS	—	CTS	CTS	CTS	4	RTSAS
Port #3/5	35	45	PGND	—	PGND	PGND	PGND	5	M5V
	36	46	RX - TX	—	TX	TXD	DTR	6	P5V
	37	47	/RX - /TX	—	/TX	RXD	DSR	7	P24V
	38	48	—	—	RX	RTS	—	8	LTG_A
	39	49	—	—	/RX	CTS	DCD	9	RTSPG

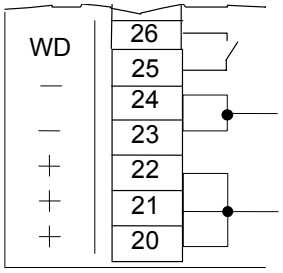
Serial data ports, sockets B1 and B2: 9-pole, D-type Port #3 and Port #5						MPI/RS 485	
D-type B1 and B2	RS 422 PCD2.F520	RS 485 PCD2.F52	RS 232 PCD2.F522	PROFIBUS	LonWorks®	MPI RS 485	
1	PGND	PGND	PGND	PGND	PGND	1	–
2	–	–	–	–	–	2	M24V
3	/TX	/RX – /TX	RxD	RxD/TxD-P	LON A	3	LTG_B
4	–	–	–	CNTR-P/RTS	–	4	RTSAS
5	RX	–	CTS	GND	LON GND	5	M5V
6	/RX	–	RTS	+5V	–	6	P5V
7	–	–	–	–	–	7	P24V
8	TX	RX – TX	TxD	RxD/TxD-N	LON B	8	LTG_A
9	–	–	–	–	–	9	RTSPG

1) PROFIBUS DP/FMS and LONWORKS®
Connection of sockets B(1) and B2 can be achieved either via screw terminal blocks or via the 9-pole D-type connector.

Details should be obtained from the relevant documentation.

7.3.4 Connection of supply, electronic fuse and noise suppression

24 VDC



The supply is connected at terminals 20 to 24 with wires of max. 1.5 mm2 (with cable end bush).

Smoothed or pulsed direct current can be used.

The "24 VDC" LED indicates when the supply voltage is present.
Reverse voltage protection prevents the destruction of the circuit by incorrect connection.
The electronic fuse takes the form of a PTC resistor (multi fuse) located in the 24 V circuit. It also prevents any fault from destroying the circuit.
Expensive interference filters keep noise voltages away from the electronic circuits (4 kV in accordance with IEC 1000-4-4).

7.3.5 Battery

This PCD is equipped with a standard, non-rechargeable 3.0 V lithium battery

- Type: CR 2032 (IEC)

A battery is enclosed with each new PCD and must be inserted before commissioning. SAIA only recommends the use of types with a capacity of min. 200 mAh, e.g.:

- RENATA order reference 4'507'4817'0

The battery must be inserted so that the positive pole (+) is visible.
The battery supports the following functions during a power failure:

- Buffering of user program memory (FC, FB, DB)
- Buffering of user data (flag, counter)
- Real-time clock

How long the battery can safeguard stored data depends largely on the power needs of RAM memory. If the calculation is based on extreme values, total buffer duration (when the PCD is isolated from the supply) is 1 to 3 years. The batteries spontaneously discharge at an annual rate of approx. 5%.
These values relate to an ambient temperature of 25°C.
The above figures are reduced at an ambient temperature of 40°C.

The Battery LED comes on and OB 81 is called whenever:

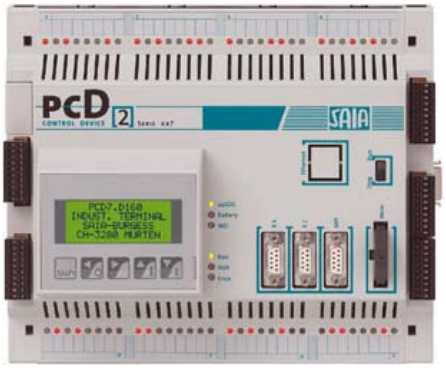
- battery power is lower than 2.4V or higher than 3.5 V
- the battery is flat
- the battery has an interruption
- the battery is missing

Changing the battery

In any operating mode the battery can be changed without difficulty and without loss of data, as long as power remains connected to the PCD2.

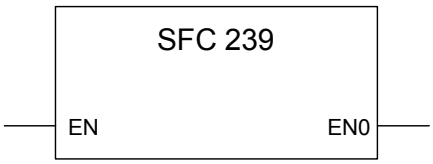
Battery Box

(Pull cover towards you to open)

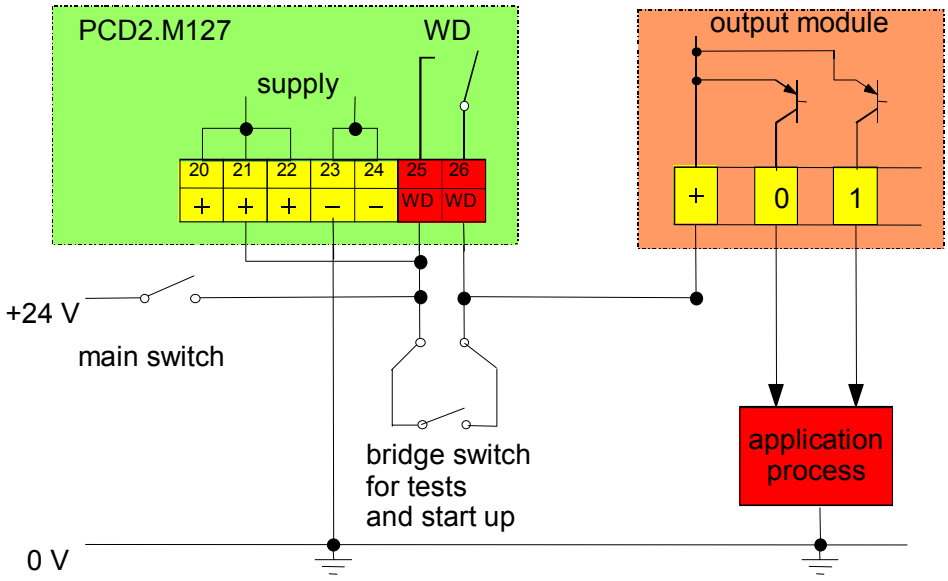


7.3.6 Watch Dog

There is a watchdog relay integrated on the PCD2-CPUs with the WD which for example, the access of the supply voltage can be controlled. After activation the watchdog must be triggered in a time of about 350ms (320...380ms) by the call up of the SFC239 (WDOG), so the watchdog-relay is kept closed. This gives a especially high security even if the PLC – processor has a fails.



Circuit example and connection allocation:

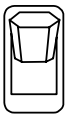


As long as the cycle time of the PLC does not exceed the 350ms (320...380ms), one call in the PLC program is enough to keep the watchdog relay closed. If the cycle time is longer it is possible to call the SFC239 more often within one PLC cycle, or if it is possible to program an appropriate cyclic interrupt OB (for example. OB35, execution all 300ms).

Caution:
The watchdog relay is using the address of the peripheral bus. No matter if it gets used or not it is not possible to use all PCD2-modules totally in the module slot 16.

7.3.7 „Run – Stop“ switch

The **RUN – HALT switch** provides a manual way of activating/deactivating the processing of a program, when necessary.



Run

Halt

7.3.8 Processor module operating states

To display there are 4 LEDs:	SUPPLY 24 VDC	LED yellow
	RUN	LED yellow
	ERROR	LED yellow
	HALT	LED red

The LED "SUPPLY 24 VDC" displays that the power supply is o.k.
The LEDs RUN, HALT and ERROR indicates different CPU-Modes:

	POST,	STOP,	ANLAUF	RUN	ERROR
	POST	**STOP**	**ANLAUF**	**RUN**	**Hard system error**
SUPPLY 24VDC	●	●	●	●	●
RUN	● / ❍	❍	✲	●	✲
ERROR	● / ❍	❍	❍	❍	✲
STOP	❍	❍	❍	❍	✲

● LED is switched on
✲: LED flashing
❍: LED is switched off

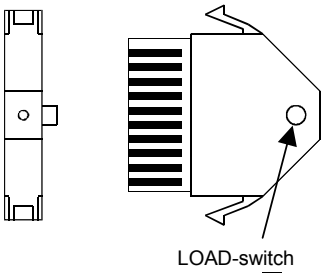
Operating modes

POST (Power On Self Test)	RUN on/off ERROR on/off SUPPLY on	Self check for approx. 5 sec By switching on
STOP	RUN off ERROR off SUPPLY on	PCD is in STOP state. The outputs are Switched off, the user program Is not executed
ANLAUF	RUN flashing ERROR off SUPPLY on	State between STOP and RUN. The start OB is executed (if existing)
RUN	RUN on ERROR off SUPPLY on	Normal processing of the user program.
bad error	RUN on/off ERROR on/off STOP on/off SUPPLY ein	System errors which can not be deleted by the user. (HW error, operating system error)

7.3.9 Flash Card PCD7.R400, 1 MByte

The user programm can be saved on the Flash Card PCD7.R400. The Flash Card can be changed by untrained Staff. The PCD-Cover doesn't have to be moved for changing the Flash-Card.

Transfer of a user program



With the PCD7.R400 flash memory card it is easy to copy any program that is stored on the card to the user memory of the relevant PCD.

If after switching on no program in the user program memory (RAM) is present the program will automaticly be transfered from the set memory module into the user program memory (RAM) and afterwards it will be started.

Manual loading of the user program

The transfer of the user program from the set Flash-Card into the user program memory (RAM) can also be done manually.

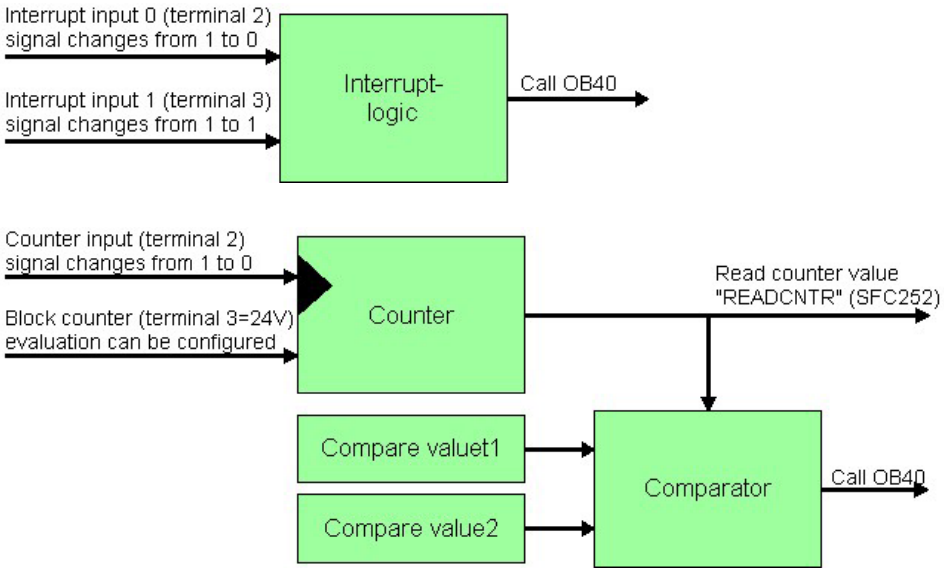
Caution:
The loading of a user program from the Flash Card will overwrite an existing program in the RAM (with all its data blocks!).

What to do:

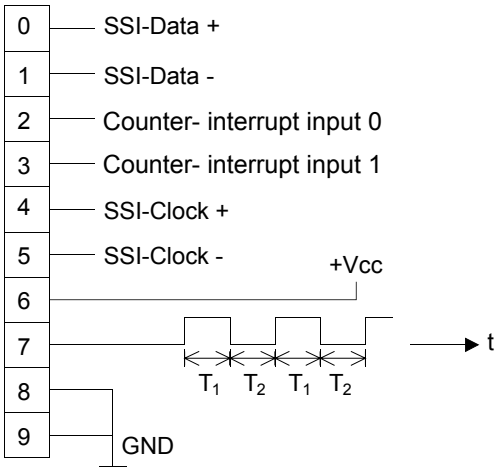
1. bring the PLC into operating status STOP
2. press the load switch for 4 seconds (preferably with the peak of a pen)
3. bring PLC into operating status RUN

7.3.10 Interrupt-input / fast counter

The interrupt input and the fast counter uses the same blocks. Because of that it is only possible to use the interrupt input or the fast counter,not both at the same time.



Allocation of the screw terminal blocks (see connection allocation).



Input signals

The different functions of the signals for the counter mode "Counter input and Counter access/ Interrupt input 0 and 1" depend on the counter mode.
Through the multiplexed functions get the signals for "Counter input and Counter access/ Interrupt input 0 and 1"depending on the operating type a different function.

External Signal	Counter mode	Interrupt mode
Counter input / Interrupt input 0	cycle	Interrupt input 0 (INT0)
Counter access / Interrupt input 1	access	Interrupt input 1 (INT1)

The inputs are made for 24-Volt-Signals.

Operating mode “Interrupt”

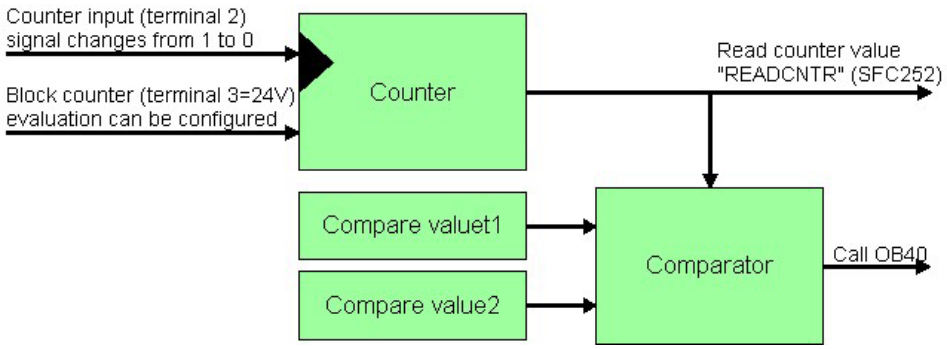
The interrupt inputs are activated like this:

- A falling edge activates the Interrupt input 0 (terminal 2)
- A rising edge actives the Interrupt input 1 (terminal 3).
- Input 0 will only cause an interrupt if input 1 = 0.

When an interrupt input is active the OB40 will be started.

Operating mode “Counter”

The counter counts the impulse of the tact-input when the access (= 0) is activ. The current Count value can be read out (SFC 252). It is possible to compare the count value with 2 compare values. Each time the compare value is reached the OB40 will be called (if accessed). The maximum number of compare values for the counter is 2. The compare value 1 must be smaller than the compare value 2. The counter counts upwards (incremented).

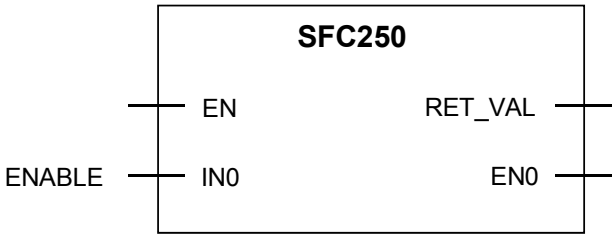


Structure and Function of the fast counter

- The counter always stars with 0(zero)
- The compare value 1 must be smaler than the compare value 2
- The counter counts only up to the compare value 2
- The counter is always counting upwards

Release/Block interrupt inputs SFC 250 "INP_INT"

With the SFC "INP_INT" the interrupt inputs get blockd or released.



Function

The SFC 250 "INP_INT" is used to block or release the interrupt inputs. It is only possible to block or access both interrupt inputs at the same time. To block or access the interrupt the SFC 250 has only to be called up once in the user program. When the interrupts are accessed and an interrupt input is activated (interrupt input 0 → falling edge, interrupt input 1 → rising edge), the OB40 is called. In local data byte "OB40_STRT_INF" it is possible to call up which interrupt input is active:

OB40_STRT_INF = B#16#41 → Interrupt input 0
OB40_STRT_INF = B#16#42 → Interrupt input 1

Parameter

With ENABLE it is possible to block or release interrupt input.
(Typ: BOOL)

- ENABLE = 1 → access interrupts
- ENABLE = 0 → block interrupts

Parameter	Declaration	Datatyp	memory-area	description
ENABLE	INPUT	BIT	E,A,M,D,L	1 → access Interrupts 0 → block Interrupts
RET_VAL	OUTPUT	WORD	E,A,M,D,L	Error information

When interrupt conditions appear the OB 40 will get called up.

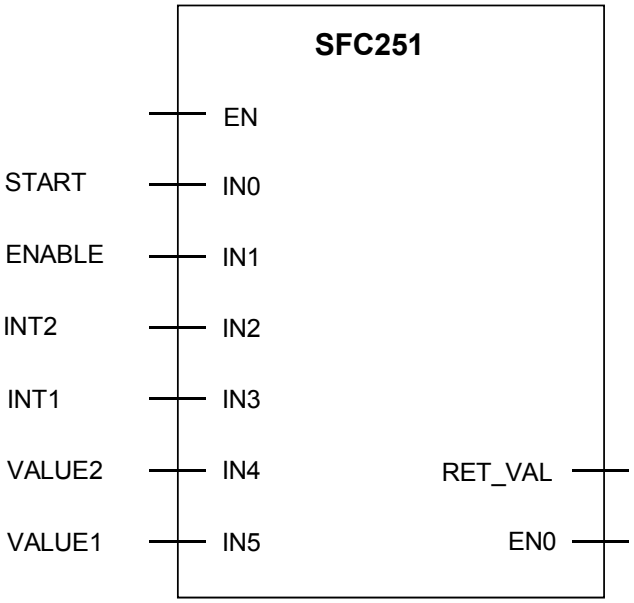
Caution:
The interrup input 1 (terminal 3) will become active at a rising edge the interrupt input 0 (terminal 2) at a falling edge. The input 1 only causes an interrupt when the input 2 = is zero

Errorinformation

none

Configure / start counter SFC 251 "INITCNTR"

With the SFC "INITCNTR" the integrated counter can be configured, started and stopped.



Function

The SFC 251 "INITCNTR" is used for initialization, starting and stopping of the integrated counter. For the configuering or starting it is only required to call the SFC 251 once in the user program.

Parameter

With **START** the counter gets started or stopped: (Typ: BOOL)

- START = 1 → Start counter
- START = 0 → Stop counter

With **ENABLE** it is possible to select if an external release signal should be evaluated: (Typ: BOOL)

- ENABLE = 1 → access will be evaluated, counter only counts if release signal = 0.
- ENABLE = 0 → release signal won't be evaluated, counter is counting always.

With **INT1** and **INT2** it is possible to start the OB40 each time a compare value is reached: (Typ: BOOL)

- INT1 = 1 → OB 40 gets started when the compare value 1 is reached.
- INT1 = 0 → OB 40 doesn't get started when the compare value 1 is reached.
- INT2 = 1 → OB 40 gets started when the compare value 2 is reached.
- INT2 = 0 → OB 40 doesn't get started when the compare value 2 is reached.

VALUE1 and **VALUE2** are the compare values with which the counter gets compared. Possible values for VALUE1 or VALUE2 are W#l6#0002 to W#16#FFFF or 0. (Typ: WORD)

Error information

After call of the SFCs it is possible to view the value that has been restored via the RFT_VAL. (Type. INT) register.

- RET_VAL = 0000h → no error
- RET_VAL = 00FEh → invalid compare value (e.g. 1)

Parameter

Parameter	Declaration	Data-typ	memory-area	description
START	INPUT	BIT	E,A,M,D,L	1 → start counter (counts up) 0 → Stop counter
ENABLE	INPUT	BIT	E,A,M,D,L	1 → Enable active input 0 → Enable inactive input
INT2	INPUT	BIT	E,A,M,D,L	1 → Interrupt when reaching the second counter value 0 → no Interrupt when reaching the second counter value
INT1	INPUT	BIT	E,A,M,D,L	1 → Interrupt when reaching the first counter position 0 → No Interrupt when reaching the first counter value
VALUE2	INPUT	WORD	E,A,M,D,L	Second counter value
VALUE1	INPUT	WORD	E,A,M,D,L	First counter value
RET_VAL	OUTPUT	WORD	E,A,M,D,L	Error information

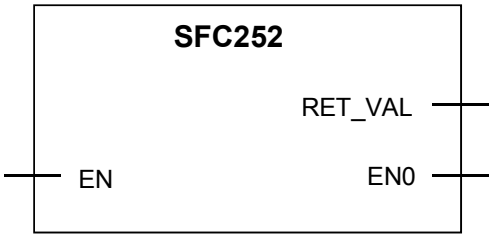
When the interrupts are released the OB40 will be called when the counter positions are reached.

Error information

Error code (W#16#....)	Description
0000	No error
00FD	Invalid counter position (this means a counter value 1 was set)

Read counterpositon SFC 252 "READCNTR"

With the SFC "READCNTR" the counter position gets read



Parameter

Parameter	Declaration	Data-typ	memory-area	description
RET_VAL	OUTPUT	WORD	E,A,M,D,L	The parameter RET_VAL contains the read value.