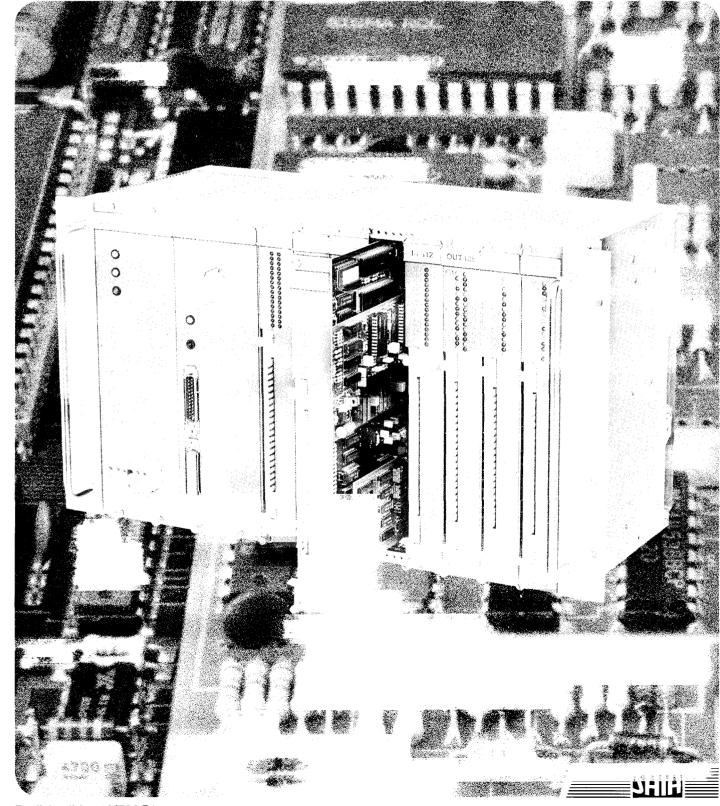


SAIA[®]PLC Programmable controllers

Manuel of the series PCA 2 Hardware



English edition 26/720 E1

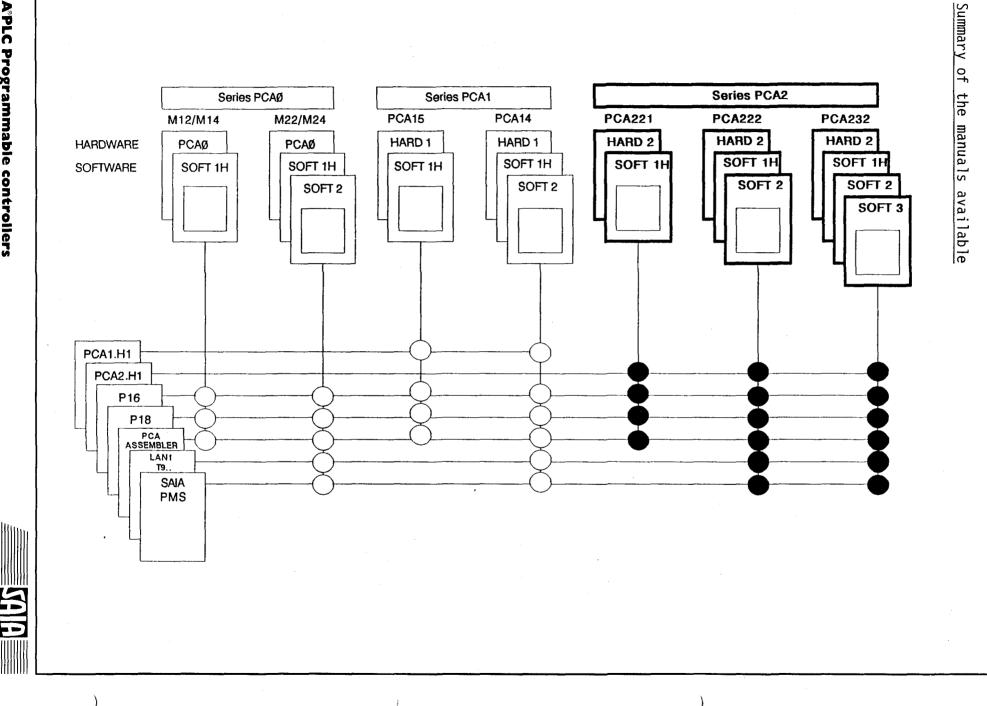
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HARDWARE - PCA2

GENERAL

- PART A HOUSING, PROCESSOR AND POWER SUPPLY MODULES
- PART B INPUT/OUTPUT MODULES as well as ADDITIONAL and DISPLAY MODULES
- PART C OPERATING MODES

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Series PCA1 Series PCAØ Series PCA2 Soft level 3 PCA232 ..C3Ø Soft level 2 + 32 word, instructions for User memory - arithmetic ± 9 digits 8K program steps M32 - data transfer + 8K text characters - word register + 8K byte data 256 or 512 I/O PCA14 Soft level 2 Standard versions and OEM PCA222 PCA141 PCA147 PCA157 + ...C45 Soft level 1H ..C3Ø PCAØ.M22 PCAG.M24 + Serial interface + Date-time + Data register + Parameter instructions .M22 ..M24 ..M41 .M47 (soft interrupt, FIFO, .M47 Ρ́ID) max. 32 I/O max. 64 I/0 256 or 512 I/0 32(56) 64(112) 128(224) 1/0 User memory User memory User memory max. 4K program steps max. 8K program steps max. 8K program steps max. 4K text characters/data max. 8K text characters/data max. 8K text characters/data PCA15 Soft level 1H Standard versions PCA221 PCA151 PCA156 PCA157 + ...C45 Instruction set with ..C3Ø 32 basic instructions for PCA0.M12 PCAØ.M14 - timers and counters - parallel programs and subroutines .M12 - indexing, etc. ..M14 ..M51 ..M56 ..M57 ..C45 20 additional instructions for 24/32 1/0 48/64 1/0 32(56) 64(112) 128(224) 1/0 256 or 512 I/0 - arithmetic - data transfer User memory User memory User memory - check-sum max. 4K program steps max. 4K program steps max. 8K program steps

Overview of the SAIA°PLC, system family PCA

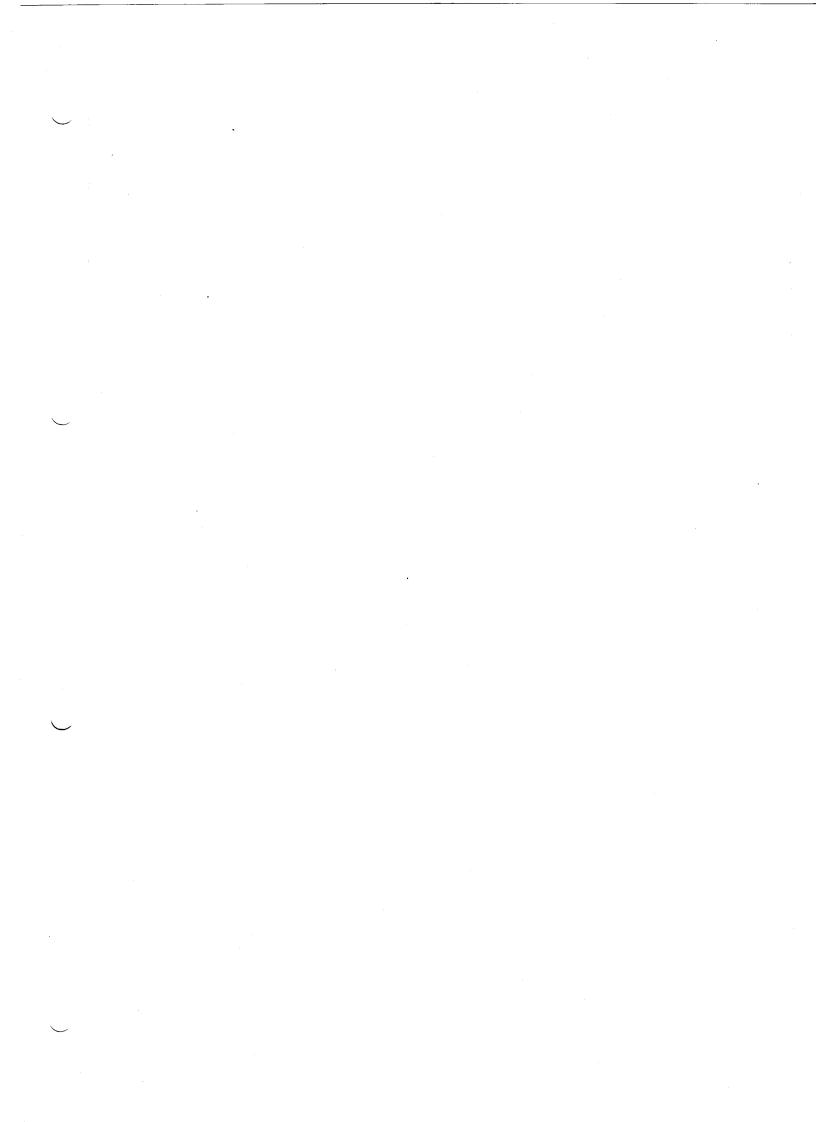


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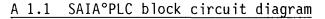
PART A HARDWARE

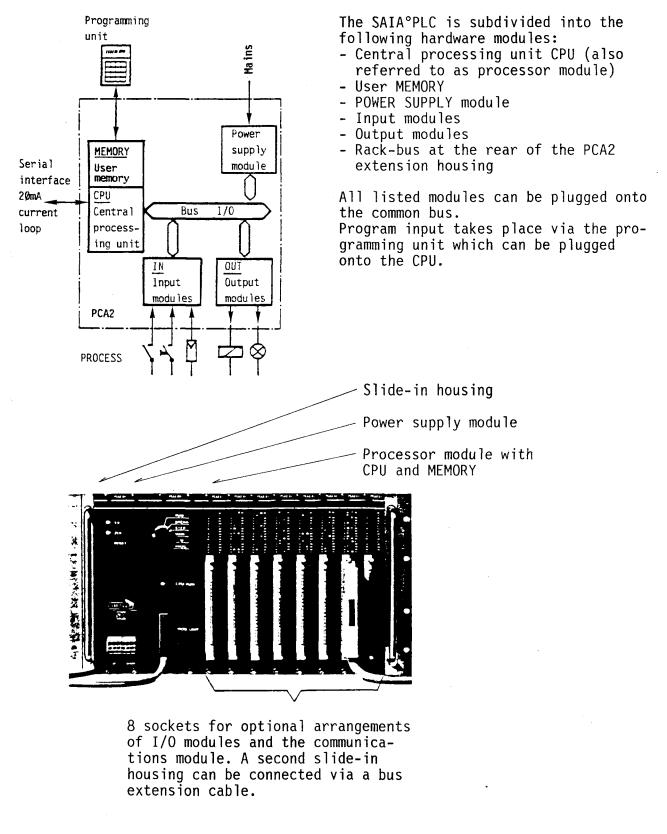
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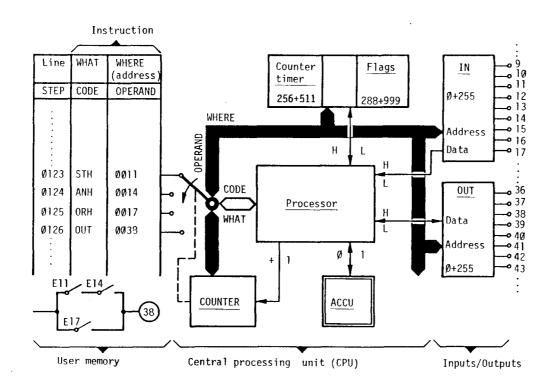
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PARTA Hardware

A 1 System structure







A 1.2 Functional description of the SAIA°PLC

The instructions for linking the input signals and formation of the actual output states are entered by the user in the user memory, arranged in "words". Each word having a length of 16 bits comprises a complete instruction, subdivided into CODE and OPERAND. The CODE states "what" is to be executed, whilst the OPERAND states "where" the element under consideration is located.

The instructions are read and interpreted consecutively by the CPU. After an instruction has been processed, the step counter is incremented by 1 and the next instruction in the user memory is read. Additionally, the logical states of the elements (H or L) are interrogated by the CPU via the data bus. The result of each logic operation is stored in the accumulator (ACCU). The results are transmitted, for example, to outputs with an output instruction.

The CPU contains all units required for auxiliary functions, such as e.g.: timer and counter registers, flag memories, index registers etc. The return address for subroutines are stored in the auxiliary registers.

SAIA

PCA2.M32			User memory 8K program lines Text memory 8K ASCII-characte Data memory 8K data of 8 bit ¹) Word processor 1K word register of Timer, counter o 256 registers of 10	ers of 8 bit ¹⁾ of 8 bit/2 digits or arithmetic rec	
PCA2.M22			User memory 48K program lin Text memory 08K ASCII-char Data memory 08K data of 8 bi Timer, counter of 224 registers of 1	acters of 8 bit ²⁾ it ²⁾	
PCA2.M21			User memory 8K program lines Timer, counter o 64 registers of 16	or arithmetic req	jister
2)		division of the entire storage capacity of 32K byte. Other divisions are however, with limitations concerning the programming units. torage capacity amounts to 16K byte, 8K byte of which can be defined of 2K bytes as user, text and/or data memory. Two sockets are available t and data memory onto which either a RAM or EPROM can be plugged.	• •		
2) Su	The total s in packets for the tex	 torage capacity amounts to 16K byte, 8K byte of which can be defined of 2K bytes as user, text and/or data memory. Two sockets are available t and data memory onto which either a RAM or EPROM can be plugged. of the performance levels and functions available Arithmetic functions in the word register: +/-/÷/×/√ / COMP, computing capacity ± 999 999 999 Data transfer in the word register 	PCA2.M21	PCA2.M22	PCA2.M3
2)	The total s in packets for the tex	 torage capacity amounts to 16K byte, 8K byte of which can be defined of 2K bytes as user, text and/or data memory. Two sockets are available t and data memory onto which either a RAM or EPROM can be plugged. of the performance levels and functions available Arithmetic functions in the word register: +/-/±/×/√ (COMP, computing capacity ± 999 999 999 	PCA2.M21	PCA2.M22	PCA2.M3

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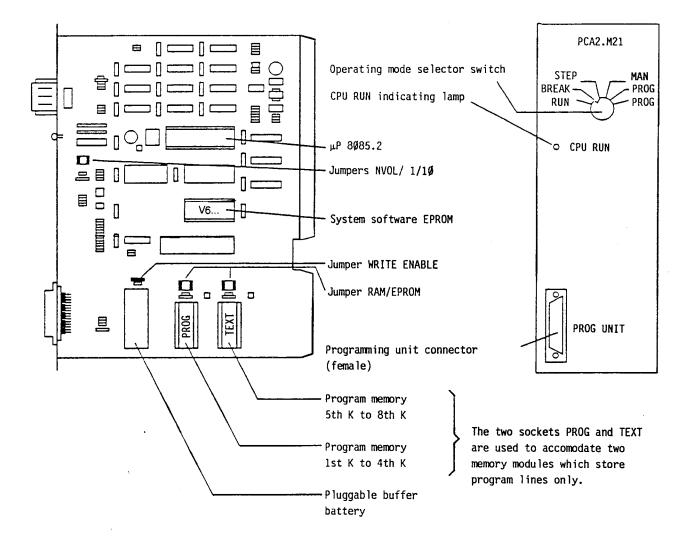
A 2 PCA2.M21 Processor module (software level (1))

<u>Technical data</u>			
CPU	μΡ 8Ø85.2, system program V6.21 ¹)		
Cycle time	7Øμs per program line (average of logic instructions)		
Instruction set	Software level 1H 32 basic instructions + 2Ø additional instructions for transfer functions, arithmetics (+, -, x, ÷) and check sum		
Parallel programs and subroutines	Up to 16 parallel programs, any number of subroutines nested down through 3 levels		
Index register	16 (1 per parallel program, capacity of 255)		
User memory	8K (4K + 4K) program lines on EPROM, RAM or buffered RAM chip on two sockets		
Inputs and outputs	256 or 512 (with extension housing 256 I + 256 O)		
Flag memory	712 flags, 235 of which are non-volatile 477 are volatile or non-volatile 2>		
Timer and counter or arithmetic registers	32 timer or counter registers + 32 counter registers, volatile ² >		
Counting or computing capacity	65'535 (2º5-1) per counter register, may be increased as desired by means of cascading		
Time range	Ø.16553s (Ø.Ø1655s) 2)		

¹) When switching on the PLC, the CPU system version is displayed on the programming unit ...PlØ or ...PØ5 for about one second.

²) Please refer to the following text for modification possibilities.

Presentation



Printed circuit board

NVOL	<u>When the jumper is inserted, all</u> flags, timer and counter registers are <u>non-volatile</u> . When the <u>jumper is not inserted</u> (standard setting) only the flags <u>765999</u> are non-volatile.
1/1Ø	<u>When the jumper is inserted</u> (factory setting), the time base for the timers is 1/1Øs. Without the jumper being inserted, it is 1/1ØØs.

A No function on the PCA2.M21.

When the jumper is not inserted, both locations are write-pro-WRITE ENABLE tected. The write lead connection for the old buffered RAM-memories (e.g. مصم R94) does not depend on this jumper. RAM Selection of the supply voltage for the user memory with the EPROM jumper inserted in: --> voltage supply by buffer battery of the processor module RAM EPROM --> direct voltage supply 64K memories are recommended as memory modules: . buffered RAM-memory PCA1.R95/R96 . RAM-chip 6264 or 8464 (order no. 4'502'4718'0) . EPROM 2764 (order no. 4'502'4719'0) When using buffered RAM-memories, the selectable jumper must be inserted in EPROM, in order not to overburden the buffer battery. It supplies the registers (counters/timers, flags, data blocks), Buffer battery date-time and, if RAM-chips 6264 or 8464 are used, this user memory, too. Data remains stored for about 2 months after switching the PLC off. Life expectancy of the NiCd-Accu is approximately 5 years (see sticker). Spare part no. 4'507'1360'0.

Front panel

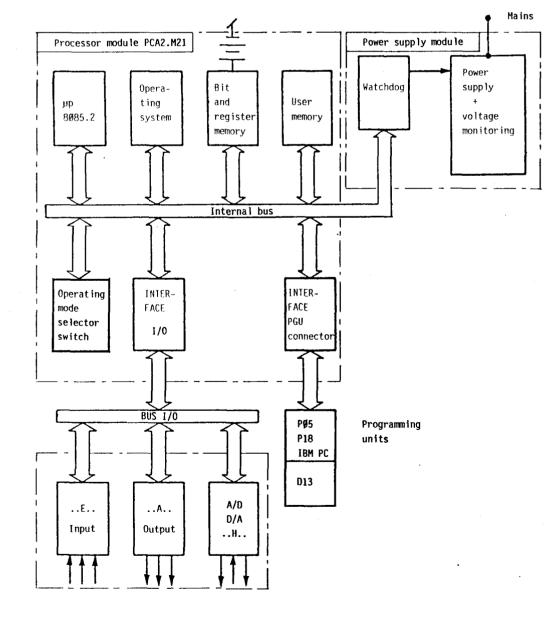
The 25-pole connector serves to connect the programming unit (PGU). The PGUconnector is female and it is fitted with a sliding lock.

<u>The "CPU RUN" indicating lamp</u> blinks every 2s during normal operation of the CPU. If the time base is changed to $\emptyset.\emptyset$ 1s, the flashing cycle is $\emptyset.2s$ (5Hz). If the lamp remains in the same state (on or off), either the power unit was not switched on, the PLC is in RESET-mode, the CPU is defective or a trap has been produced in the software sequence.

The operating mode selector switch mainly serves for starting up and troubleshooting. If the programming unit is disconnected, the <u>operating mode is</u> <u>always "RUN"</u> independent of the position of the rotary switch.

The two PROG positions have the same function.

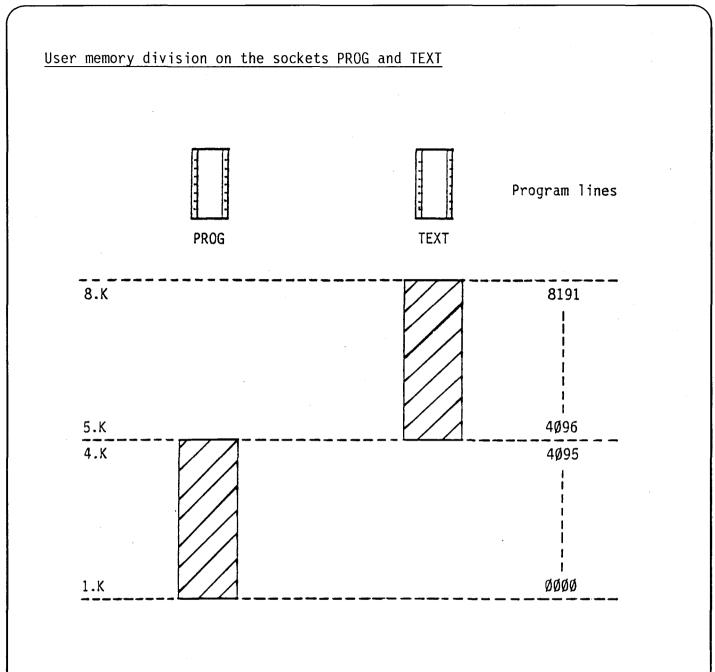
<u>Block circuit diagram</u>



Register organisation Register 1 bit 16 bits Element address 999 F Flags (NV) 765 8 bits 764 PP 15 IR F Flags Index registers (VOL*) (V) PP Ø 32Ø 319 F/C Flags (VOL*) Counters С Counters (VOL*) 288 287 C/T Counters (VOL*) Timers T Timers (VOL*) 256 255 I/O Inputs (V) Outputs øøø (V) volatile (NV) non-volatile (VOL*) volatile, can be made non-volatile with jumper NVOL

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The sockets PROG and TEXT accomodate the memory modules (RAM or EPROM) in which only user programs are stored.

<u>Technical data</u> CPU	μ D QAQE 2 suctom program V6 2 1)
	μP 8Ø85.2, system program V6.2 1)
Cycle time	7Øμs (per program line, logic instructions)
Instruction set	32 basic instructions, 20 additional in- structions for arithmetic, text output, communication and parameter functions
Parameter functions	PID-loops, shift registers, check sum, interrupt management
Number of parallel programs	16 (PP 15 for interrupt control)
Number of index registers	16 (1 per parallel program, capacity of 255
Number of subroutines	as desired, in max. 3 levels each
User memory (16 bits)	max. 8K program lines in EPROM, RAM or buffered RAM memory on two sockets
Text memory (8 bits)	max. 8K characters in EPROM, RAM or buffered RAM memory
Data memory (8 bits)	max. 8K characters in EPROM, RAM or buffered RAM memory
Inputs and outputs	256 or 512 (with extension housing 256 I + 256 O)
Flags	712 (477 volatile ²), 235 non-volatile)
No. of timers	32 (ADD 256287)
No. of counters or arithmetic reg.	224 (ADD 256479) as of V6.23Ø
Counting cap. or arithmetic reg.	65'535 (2 ¹⁶ -1) with cascading as desired
Time range	Ø.1 (Ø.Ø1)s6553 (655)s 2)
Date-time (hardware)	Week, day of the week, year, month, day, h, m, s
Accuracy of date-time	higher than 15s per month (details see module PCA2.R27)
Power reserve of date-time	2 months at 25°C (when user memories EPROM or R95/R96 are used)
Serial data interface	20mA current loop, active or passive, for input/output of text or communication acc. to DIN 66019, baud rate 1109600 bauds ³

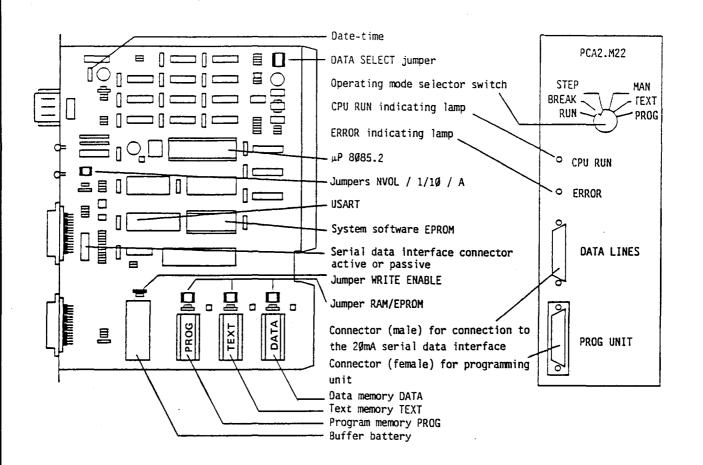
when switching on the PLC, the system version is displayed on the programming unit PL second. For this reason, the operating mode selector switch must be in position RUN.
 Please refer to the following text for modification possibilities.
 High baud rates require an appropriate program structure.

5

10A

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Presentation



Printed circuit board

NVOL	<u>When the jumper is inserted, all</u> flags, timer and counter registers are <u>non-volatile</u> . When the jumper is not inserted (standard setting) only the flags <u>765999</u> are non-volatile.
1/1Ø	<u>When the jumper is inserted</u> (factory setting), the time base for the timers is 1/1Øs. <u>Without the jumper being inserted</u> , it is 1/1ØØs.
A	<u>When the jumper is inserted</u> , all 32 data blocks (PID) are <u>volatile</u> (factory setting).

DATA-SEL	The total storage space available for text and data memory <u>together</u> amounts to max. 8K bytes (8K characters). Memory areas can be assigned to the <u>DATA socket</u> by inserting the jumpers.
	The TEXT socket as well as the DATA socket can be used to accomo- date RAM- or EPROM-memories for the user program in the range 4Ø968191.
	Arrangement of the sockets and memory areas see chapter "User memory division".
WRITE ENABLE ∽ <u>~~</u>	If a RAM is used on sockets PROG and TEXT, the write lines need to be connected separately by <u>inserting</u> the jumper. When the <u>jumper is not inserted</u> , write-protection is provided on both sockets. The DATA socket is not write-protected. Write lead connection for the old buffered RAM-memories (e.g. R94) does <u>not depend on this jumper</u> .
RAM EPROM	Selection of the supply voltage for the user memory with the <u>jumper</u> <u>inserted</u> on:
s 2	RAM> voltage supply by buffer battery EPROM> direct voltage supply
	64K memories (8K bytes) are recommended as memory modules:
	. buffered RAM-memory PCA1.R95/R96 . RAM-chip 6264 or 8464 (order no. 4'502'4718'0) . EPROM 2764 (order no. 4'502'4719'0)
	When using <u>buffered RAM-memories, the selectable jumper</u> must be <u>inserted in EPROM</u> , in order not to overburden the buffer battery.
Buffer battery	It supplies the registers (counters/timers, flags, data blocks), date-time and, if RAM-chips 6264 or 8464 are used, this user memory, too. Data remains stored for about 2 months with the PLC switched off.
	Life expectancy of the NiCd-Accu is approximately 5 years (see sticker). Spare part no. 4'507'1360'0.
Serial data	Depending on the connector position the serial data interface (20mA-current loop) can be programmed as follows:
interface	ACTIVE> active current loop (20mA for transmitter and receiver are supplied by M22)
Active	PASSIVE> passive current loop (20mA for transmitter and receiver must be supplied externally)

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Front panel

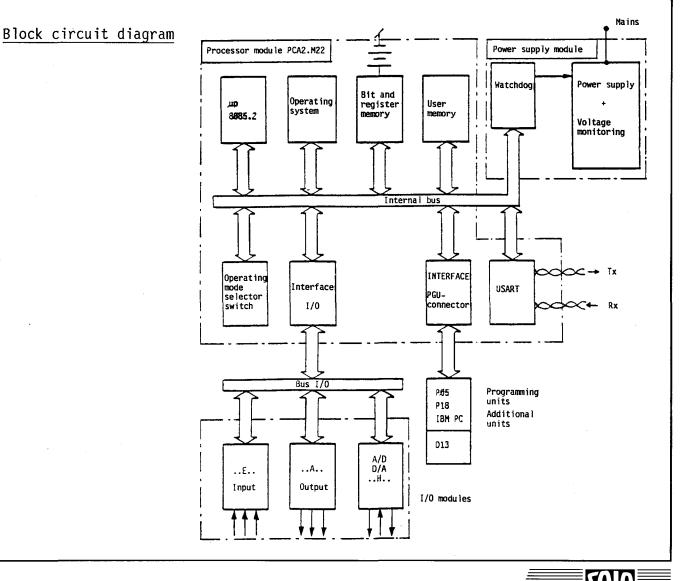
The lower connector of the two 25-pole connectors (PGU) serves to connect the programming unit. It is fitted with a sliding lock for fixing the cable connector.

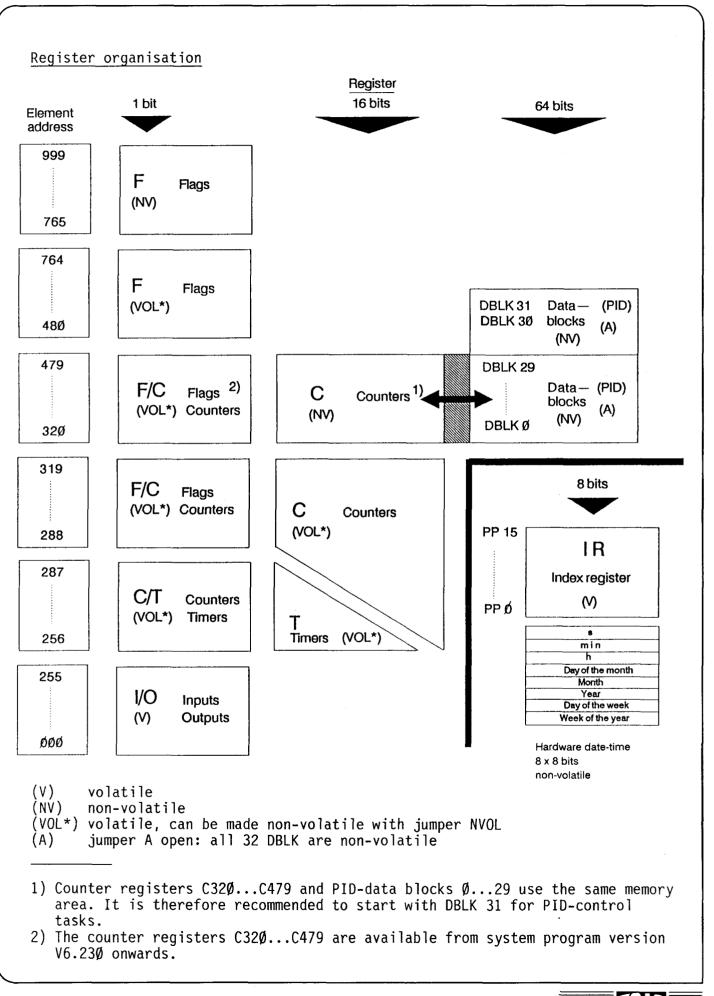
<u>The upper connector (DATA LINES)</u> is used to connect a peripheral unit. The cable connector is fastened with screws. In order not to confuse the two connectors, the PGU-connector is female and the DATA LINES connector is male. (details see M32)

<u>The "CPU-RUN" indicating lamp</u> blinks every 2s during normal operation of the CPU. If the time base is changed to $\emptyset.\emptyset$ 1s, the flashing cycle is $\emptyset.2s$ (5 Hz). If the lamp remains in the same state (on or off), either the power unit was not switched on, the PLC is in RESET-mode, the CPU is defective or a trap has been produced in the software sequence.

The "ERROR" indicating lamp indicates transmission errors in the serial data line.

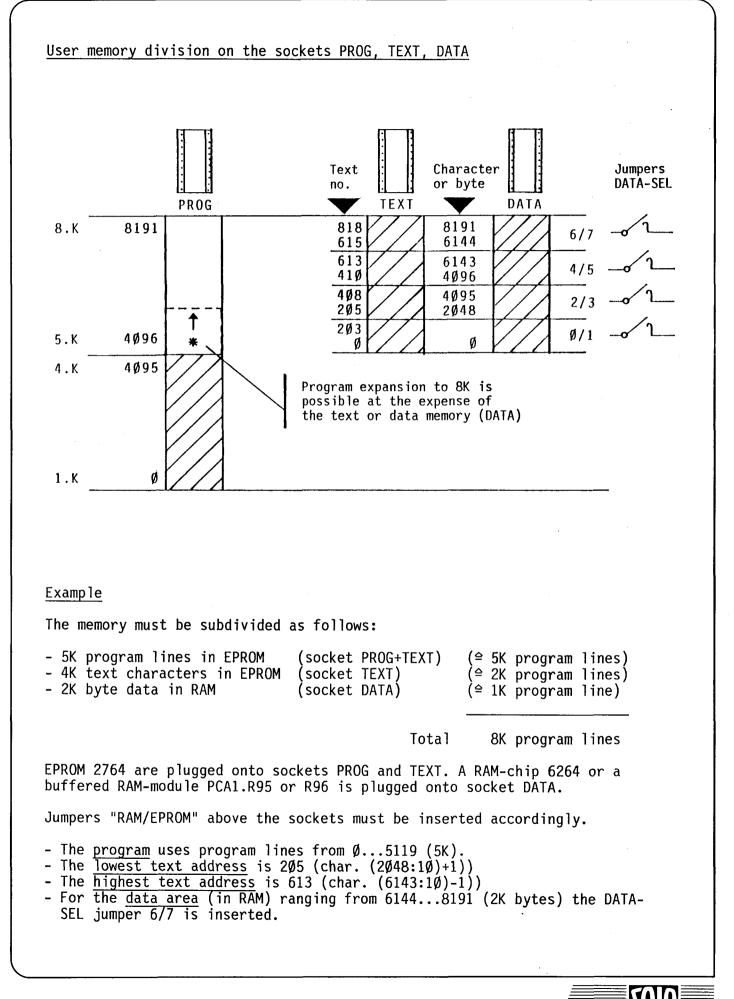
The operating mode selector switch mainly serves for starting up and troubleshooting. When the programming unit is disconnected, the <u>oprating mode is</u> <u>always "RUN"</u> independent of the position of the rotary switch.





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SAIA®PLC Programmable controllers

A 4 PCA2.M32 Processor module (software level (3))

Technical data CPU 16 bit μ P, type 68000, with system program V7.1XX 1) 35µs per program line (logic instructions) Cycle time Instruction set 32 bit instructions plus extension (arithmetic, text output, communication and parameter instructions) plus 32 word instructions Number of parallel programs 16 (PP15 for interrupt control) 16 (1 per parallel program) Number of index registers Capacity of index registers 1Ø23 (1K) Number of subroutines as desired, in max. 3 levels each in RAM or EPROM User memory 8K program steps with memory modules +8K ASCII character PCA2.R26/R27 text memory +8K byte data memory Input plus output 256 (256 I + 256 0 = max. 512 I/0 with extension)addresses housing) Software timers plus 256 (ADD 256...511) counters or arithmetic (ADD 256...287 timers/counters) registers (ADD 288...511 counters or arithmetic registers) Counting capacity $65'535(2^{16}-1)$ Time range Ø.1 (Ø.Ø1)s...6553 (655)s ²) Non-retentive and 477/235 * (ADR 288...999) retentive flags 1K byte (ADD Ø...999) non-volatile Word register Date-time, software week of the year, day of the week, year, month, day, h, min, s (without power reserve) Date-time, hardware (R27) week of the year, day of the week, year, month, day, h, min, s (with power reserve) Serial interface 20mA current loop (active or passive) Copying possibilities of RAM/EPROM/EPROM/RAM/RAM with comparison of contents user memory

1) Upon switching on the PLC, the system version is displayed on the P10 or P05 programming unit for approx. 1 second (operating mode selector switch in position RUN).

2) For possibilities of modification refer to the following text.

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Presentatio	<u>on</u>
	Buffer battery for flag memory and register RAM-memory for flag memory and register EPRON with system program 16 bit µP 68.000 Operating mode selector switch USARI Flasher for CPU RUN Indicating lamp ERROR Jumpers for time base, non-volatile flags and hardware date-time (RZ7) Connector for programming the serial data interface Connector (male) for connection to the 20mA serial data inter- face Connector (female) for pro- gramming unit Main memory location
Printed cir	Copying memory location
The pc-boar	rd accomodates all active parts of the CPU. Various properties of the modified by reinserting jumpers or plugging connectors into differ-
□ 1/1∅ □	With the jumper inserted (as delivered) the time base is 1/10s. With the jumper not inserted the time base is 1/100s.
U VOL D	<u>With the jumper inserted</u> (as delivered) the distribution of the non-retentive flags is as follows: 288764 <u>non-retentive</u> flags, volatile 765999 flags, non-volatile 256511 timer and counter register, <u>volatile</u> When the jumper is not inserted, all memory addresses from <u>256999</u> are non-volatile flags resp. timer and counter registers.
□ R27 □	<u>With the jumper inserted</u> the hardware date-time on module PCA2.R27 is recognized as master. R27 must be on the main memory socket. <u>When the jumper is not inserted</u> , the software date-time of the CPU system quartz is recognized as master (without power reserve).
	Attention : if any other memory module than R27 or R29 is on the main memory socket and the jumper R27 is inserted, the step adress 0 can be falsified in the case of RAMs.
Programming	g of the serial interface (active or passive)
	<u>Connector in the upper half</u> results in a <u>passive</u> 20mA current loop (20mA for transmitter and receiver must be supplied by an external power source). <u>Connector in the lower half</u> results in an <u>active</u> current loop (20mA for transmitter and receiver are supplied by the M32).

SAIA®PLC Programmable controllers

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SAIA

The buffer battery (NiCd accumulator) supplies all elements defined as nonvolatile (such as flags, counters, timers, word registers and data blocks) with power. Data remains stored for about 2 months. Life expectancy is approximately 5 years (see red sticker). Spare part no. 4'507'1195'0.

Front panel

The lower connector of the two 25-pole connectors (PGU) serves to connect the programming unit. It is fitted with a sliding lock for fixing the cable connector.

The upper connector (DATA LINES) is used to connect a peripheral unit. The cable connector is fastened with screws.

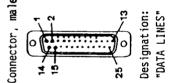
In order not to mix the two connectors, the PGU-connector is female and the DATA LINES connector is male.

The indicating lamp "CPU RUN" flashes every 2s during normal operation of the CPU. If the time base is changed to $\emptyset.\emptyset$ 1s, the flashing pulse is $\emptyset.2s$ (5 Hz). If the lamp remains ON or OFF, either the power supply unit was not switched on, the PLC is in reset position, the CPU is defective or a trap has been produced in the software sequence.

<u>The indicating lamp "ERROR"</u> indicates errors occuring along the serial data line.

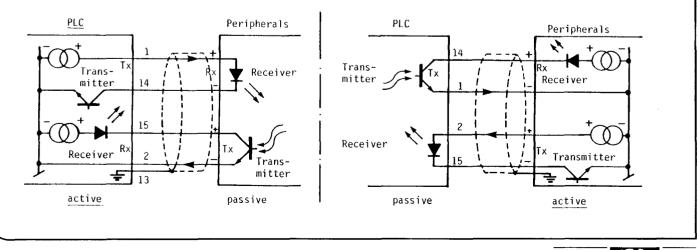
The operating mode selector switch mainly serves for starting up and troubleshooting. When the programming unit is not connected, the operating mode <u>"RUN"</u> is always selected irrespective of the rotary switch position.

Serial interface connection (only valid for PCA2.M22 and M32)

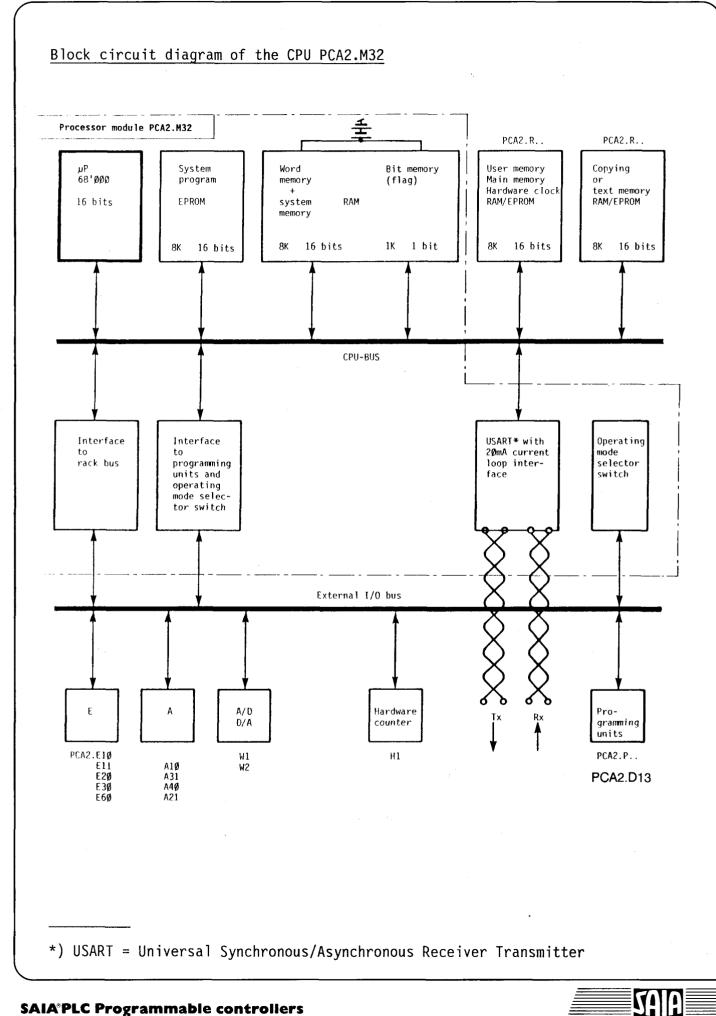


25-pole D-sub connector with locking screws

For PCA2.M22 and M32, the interface can be made "active" or "passive" and thus adapted to the peripheral unit by repositioning a multi-way connector.



SAIA®PLC Programmable controllers



SAIA[®]PLC Programmable controllers

19A

Organisation of the bit and word registers

Apart from the registers of the bit processor, the CPU PCA2.M32 comprises also a large word register to which the word processor has access.

Registers of the bit processor:

These three registers are upwards-compatible among the other SAIA°PLC of the series PCA1 and PCA2. The extended bit processor instruction set of the CPU M32, however, allows a much more extensive data exchange.

Apart from the non-volatile flags (765...999) all registers of the bit processor are volatile. All flags and counter registers can be made non-volatile by removing a jumper (see "Printed circuit board").

- Bit register En All logic states of all elements (except inputs) are stored in here. Addressing can be effected from Ø...999.
- Counter register Cn

Via the element addresses 256...511, the bit processor instruction set allows access to the counter resp. timer register of 256×16 bits (= $256 \times 65'535$). The memory is organised in binary format. The instruction set, however, allows inputs and outputs converted into decimal values resp. BCD-format.

- Index register IR (address indexing see software) The 16 registers are automatically selected via assignment of the respective parallel program. The number of 10 bits allows input and output of decimal values from Ø...1023.

Register of the word processor:

The entire word register is non-volatile. Rn words of 8 bit can be addressed from \emptyset ...999. Additional commands also allow simultaneous processing of register blocks of 5 x 8 bits. Basically, it is a register for BCD-coded values, since all arithmetic operations, preceding sings (+/-) included, are based on BCD-format. Purely binary words, however, can also be transferred and stored.

The registers \emptyset ...2 \emptyset are reserved for special functions. It is recommended not to use addresses below R5 \emptyset or R1 $\emptyset\emptyset$ for general purposes.

 $R\emptyset...R14$ are referred to as arithmetic registers, because the arithmetic operations are performed between the register blocks A $\emptyset...A2$. R4 for 2-digit and A \emptyset for 9-digit decimal numbers plus preceding signs (+/-) take precedence. The significance of the positions is evident from the following figure.

The data of the internal software date-time is stored in R15 to R19. From $R2\emptyset$ to Rn an 8-bit shift register can be created.

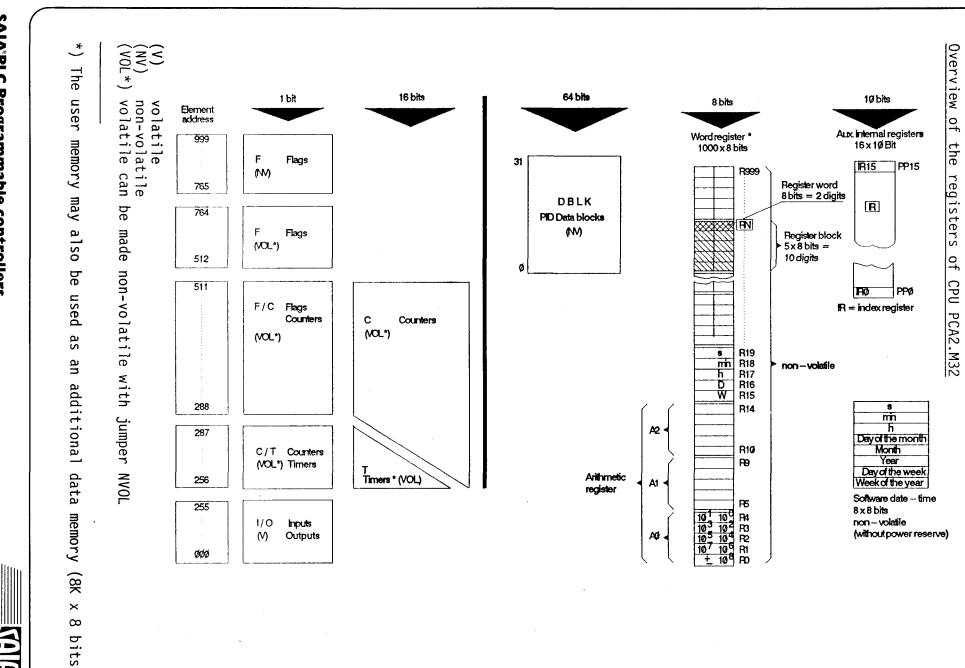
Data block register:

It serves for storing the parameters for the 32 PID-control loops and is operated with the instructions PAS $2\emptyset\emptyset$...212.



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1

Organisation of the user memory

All RAM- or EPROM-modules, except R11R12, can be used for storing user programs as well as texts and data. The full storage capacity, however, is only obtained, if memory modules PCA2.R26/R27 are used.

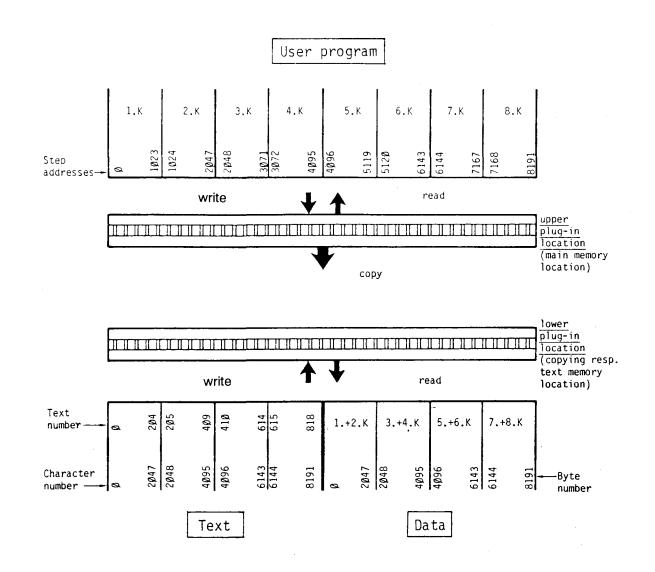
<u>The upper plug-in location</u> (main memory location) of the CPU is used for <u>user</u> programs in the address range \emptyset ...8K program steps. Module R29 with hardware date-time is also used on this socket.

The lower plug-in location can be used for texts or data. The text memory capacity is 8K ASCII-characters, the data memory capacity is 8K times 8 bits.

The detailed organisation of the user memory regarding user programs, texts and data is evident from the following figure.

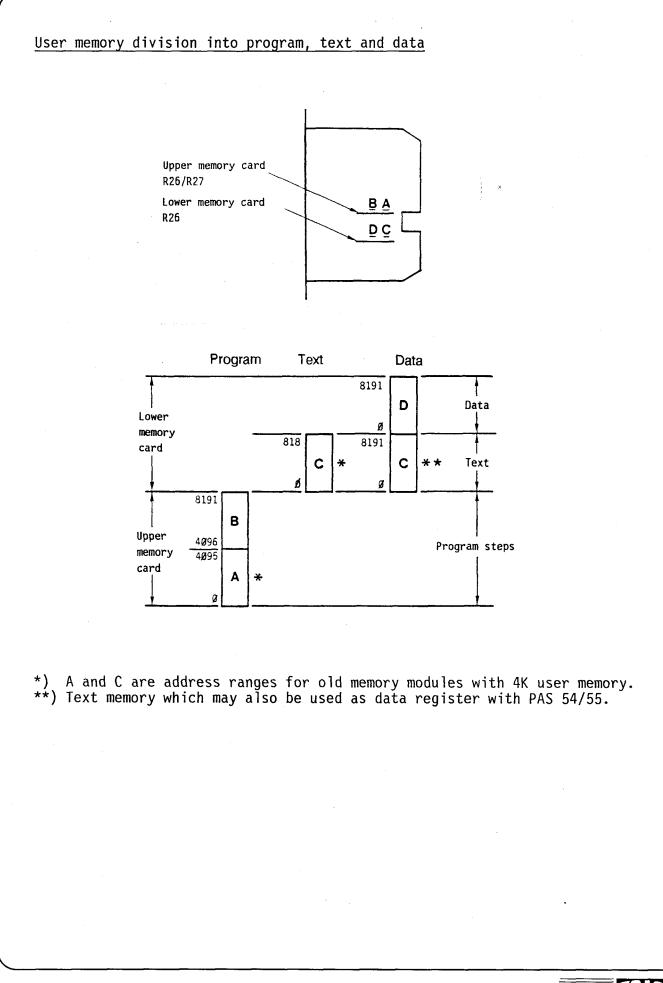
All programs resp. texts are programmed and read in the plug-in location assigned to them. Only copying to RAM or EPROM is always effected from the upper to the lower socket. If, for example, programs of more than 4K or texts are to be copied, the master card is attached at the top. Copying is effected word by word from the upper socket to the lower socket, irrespective of the contents of the memory card.

Overview of the user memory



The step addresses from the 5th K to the 8th K of the user program as well as the entire data memory of 8K bytes can be made full use of only with the memory modules PCA2.R26/R27, as the storage capacity of all other R-modules amounts to max. 4K step addresses.

If the 8K step addresses for the user program or the 8K characters for the texts are not sufficient for your application, please ask for our special documentation on possibilities of expansion.



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A 5 User memory modules

<u>Type PCA2.R26 Memory module</u> <u>Type PCA2.R27 Memory module with buffered date-time (clock module)</u>

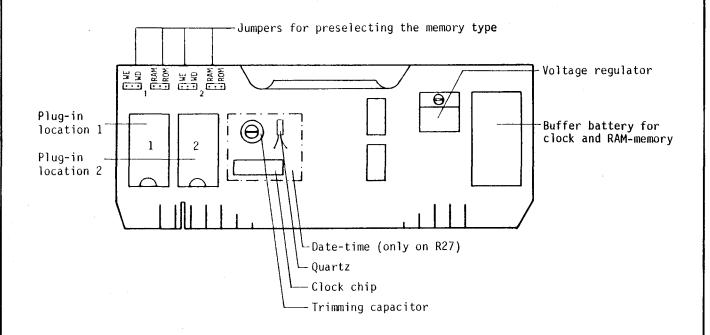
With the <u>memory module R26</u> the EPROMs 2764, the buffered RAM-module PCA2.R95 or R96 as well as the RAM types 6264 and 8464 can be programmed and read. Two of these memories can be plugged onto the module, which results in a capacity of 8K program steps.

As memory module ..R27 is identical to ..R26. The date-time incorporated in addition permits precise output of second, minute, hour, day of the month, year, day of the week, week of the year. Deviation is less than 15s per month and the power reserve exceeds 2 months. As a result, exact time switch functions as well as event or alarm loggings with date and time can be realised.

This buffered date-time module can only be evaluated with CPU PCA2.M32 on the upper socket.

Presentation

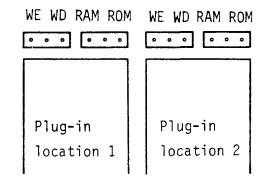
The following figure shows the clock module PCA2.R27. Next to the two memory sockets is the date-time.



The clock and any RAMs have a power reserve of more than 2 months.

Preselection of the memory type

Two jumpers are provided for each socket allowing preselection of the user memory.



The jumpers on the right RAM/ROM serve to preselect the memory type.

EPROM 2764	:	RAM ROM	The connection with the buffer battery is interrupted
PCA1.R95/R96	:	<u> </u>	butter battery is interrupted
RAM 6264, 8464	:		The RAM is buffered by the battery

The jumpers on the left WE/WD serve to determine whether the memories RAM 6264, 8464 and the buffered RAM-module PCA1.R95/R96 are write-protected or not.

Write Enable	:	WE WD	Overwriting is possible (not write-protected)
Write Disable	:		Overwriting is impossible (write-protected)

When copying EPROMs or RAMs (operating mode LCM) the jumper must be in position WE.

This structure has the following advantages:

- The user program can be divided as follows: e.g. 4K stored in an EPROM and 4K in a RAM.
- The texts of at most 8K ASCII-characters can be stored e.g. in an EPROM, while data (8K bytes) can be stored in a RAM.
- Each socket can be write-protected individually.



Buffer battery

In case of voltage failure, or when the memory module is removed, the buffer battery supplies the RAM user memories (6264 or 8464) and the date-time on module R27. Data is buffered for approx. 2 months and it has a life expectancy of 5 years. Spare part no. 4'507'1360'0.

Data and operation of clock module R27

Access to the date-time is possible only via CPU PCA2.M32 (jumper "R27"). Thus, the following functions are possible:

- Setting the clock via user program (see PAS 5Ø) or via programming unit (see C2.2).
- Output of time and/or date for logging purposes.
- Switching functions depending on date and time.

Every second the system program of the PCA2.M32 automatically transmits the contents of the date-time to the CPU. Via the user program the contents can be read out or adjusted (see PAS $5\emptyset$) at any time.

- Power reserve	> 2 months	
- Deviation	< 15 s / month (15	53ذC)
- Clock values	Week of the year Day of the week Year Month Day of the month Hours Minutes Seconds	Ø153 2) 4) Ø107 2) 3) ØØ99 Ø112 Ø128, 29, 3Ø, 31 1) ØØ23 ØØ59 ØØ59

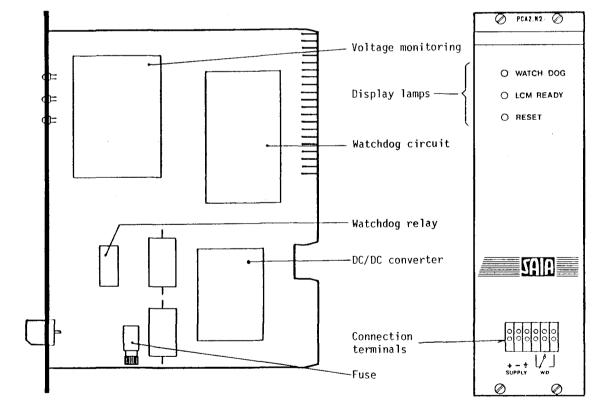
1) The date-time takes the various months and leap years into account.

²) When setting the clock it must be ensured that day and month resp. day of the week and week match. The clock does not automatically make any corrections.

³⁾ Day of the week \emptyset 1 stands for Monday, \emptyset 7 stands for Sunday.

⁴) According to the ISO-standards the first week of the year is represented by "Ø1", if January 1st is a Monday, Tuesday or Wednesday. When a new year starts, the week number has to be checked accordingly.

A 6 Power supply modules A 6.1 Type PCA2.N2Ø/N21 Power supply module for 24VDC with integrated voltage monitoring and watchdog Technical data Supply voltage V_{in} 24VDC (smoothed or pulsating) Voltage tolerance -2Ø% / +25% Power consumption (24 VDC) max. 2.5A (N2Ø) resp. 3.5A (N21) Input circuit fuse 2.5A slow-blow (N2Ø) resp. 4A slow-blow (N21) Output voltage V_{aout} (electronics) 5V stabilised $(\pm 3\%)$ Output current 5V max. <u>4A (N2Ø)</u> resp. <u>6A (N21)</u> Input voltage - 2V (at 1A) Aux. output voltage V_{aout} (EPROM) Output current 24V (Iaout) max. 1A Watchdog frequency \geq 5Hz Watchdog contact max. Ø.5A, 48VAC or VDC IP 20 or IP 30 (with terminal lid which Supply terminal protection is supplied with every extension housing) Presentation



Description

Module PCA2.N2Ø supplies a stabilised 5V for supplying the electronics unit and a non-stabilised 24V for the <u>internal</u> driving of the output circuits and the LCM function (only for PCA2.M32). The supply module output circuits are galvanically connected to the input.

An input filter is fitted to provide effective suppression of interference voltages from the 24VDC supply. Good earthing at the terminal enhances the efficiency of this protective element.

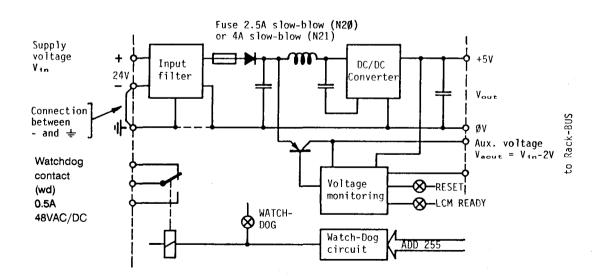
The correct function of the mains unit is monitored by several circuits and the relevant states are displayed on the front panel.

- <u>The red lamp RESET</u> lights up when the input voltage is much too low or when the 5V for the electronics is incorrect. In both cases, the processor is stopped, all elements reset (with the exception of retentive memories), and the watchdog relay is released.
- The yellow lamp LCM READY lights up, when the auxiliary voltage $V_{aout} = 24V$ to 26V ($V_{in} = 26V$ to 28V). The LCM lamp must also light up, if EPROMS 2716 are to be copied. For programming large-scale integrated EPROMS (2732A or 2764) which require a voltage tolerance of only $\pm \emptyset.5V$, module N3 \emptyset /N31 must be used.

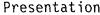
- <u>The yellow lamp WATCHDOG</u> indicates that the watchdog relay is energised. This is the case when the watchdog circuit is activated in a cycle of ≤Ø.1s by complementation of PLC address "255". The required instruction in the user program is "COO 255" which is programmed at the beginning of a <u>circulating</u> main or parallel program. The watchdog circuit thus reliably monitors continuous processing of the user program.

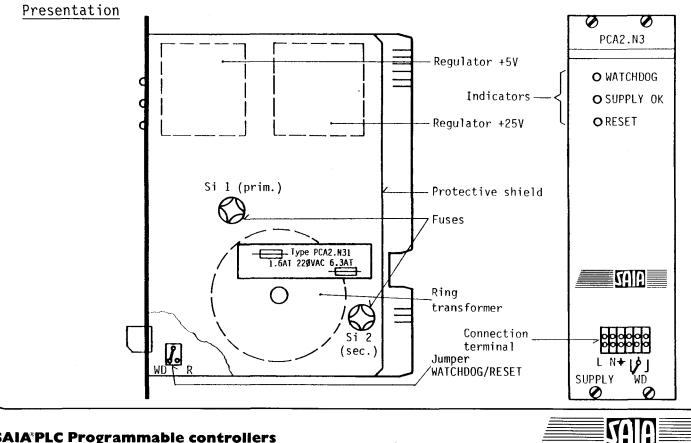
If the PLC normally processes all programs in the operating mode "RUN", the watchdog relay remains energised; in any other mode or in the event of a fault in the CPU or the supply, the relay is released. The watchdog relay is also released when the mode switch is moved from the operating mode "RUN", and the programming unit is plugged in. Appropriate safety measures can be taken using the available two-way contact.

Block circuit diagram



	<u>supply module for alternating voltage with a</u> -in voltage monitoring system and watchdog
Technical data	
Mains voltage V _{in}	22ØV, 5Ø – 6ØHz, type D4 24ØV, 5Ø – 6ØHz, type D6 11ØV, 5Ø – 6ØHz, type C8
Voltage tolerance	-15% / +1Ø%
Power consumption	8ØVA (N3Ø) resp. 12ØVA (N31)
Fuses	see below
Output voltage (electronics)	+5V stabilized
Output current 5V	max. <u>4A (N3Ø)</u> resp. max. <u>8A (N31)</u>
Output voltage (EPROM)	+25V stabilized (±1%)
Output current 25V	max. Ø.4A (N3Ø and N31)
Watchdog frequency	≥ 5Hz
Watchdog output contact	max. Ø.5A, 48VAC/VDC
External reset input	By repositioning a jumper from WD to R
Protection of the supply terminals	IP 2Ø resp. IP 3Ø (with terminal lid which is supplied with every rack unit)





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Structure

The modules N3Ø/N31 are mounted on 2 plates. The heavy transformer is mounted on the iron shield, the electronic system with the regulators is on the printed circuit board. Thus, not only good heat dissipation is achieved, but also protection against shocks, as the iron shield is additionally supported in two guideways. When transporting a PCA2, the power supply module must be removed from its plug-in location and packaged separately.

Fuses (cartridges 5 x 20 mm)

Mains (22ØV): Si 1: 1.6A slow-blow (N3Ø), 1.6A slow-blow (N31) Secondary : Si 2: 4A slow-blow (N3Ø), 6.3A slow-blow (N31)

Easy access to the fuses on the shield is provided by removing the module.

Description

The power supply module meets the <u>internal</u> power requirements of the PCA2. The input and output circuits are supplied by an <u>external power supply unit</u> operated by the user. For the PLC-modules a simple single-phase transformer with bridge rectifier is sufficient. The power supply module provides two stabilized voltages:

+ 5V for the power requirements of the electronics
 +25V for programming the EPROMs and for the <u>internal</u> activation of the output circuits.

Proper functioning of the mains unit is supervised by several circuits and the respective states are displayed on the front panel:

- <u>The red lamp RESET</u> lights up, if the mains voltage V_{in} is much too low or if the 5V-voltage falls below 4.7V. In both cases, the processor is stopped, all outputs are reset and the watchdog relay is released. The same reset is effected when the RESET-input is connected to ground ($\emptyset V$).
- <u>The yellow watchdog lamp</u> indicates that the watchdog relay is excited. This is the case when the watchdog circuit is activated in a cycle of ≤ Ø.1s by complementing the PLC-address "255". The necessary instruction in the user program is "COO 255". It is programmed at the beginning of a <u>circulating</u> main or parallel program. The watchdog circuit is used to supervise permanent execution of the user program reliably.

If the PLC executes all programs in the operating mode "RUN" normally, the watchdog relay remains excited. In a different operating mode or if a malfunction occurs in the CPU or the power supply, the relay is released. The watchdog relay is released, too, if the operating mode RUN is quit with the programming unit connected. The respective safety precautions can be taken by using the available two-way contact.

- <u>The yellow lamp SUPPLY OK</u> lights up, if both voltages +5V <u>and</u> +25V are correct.

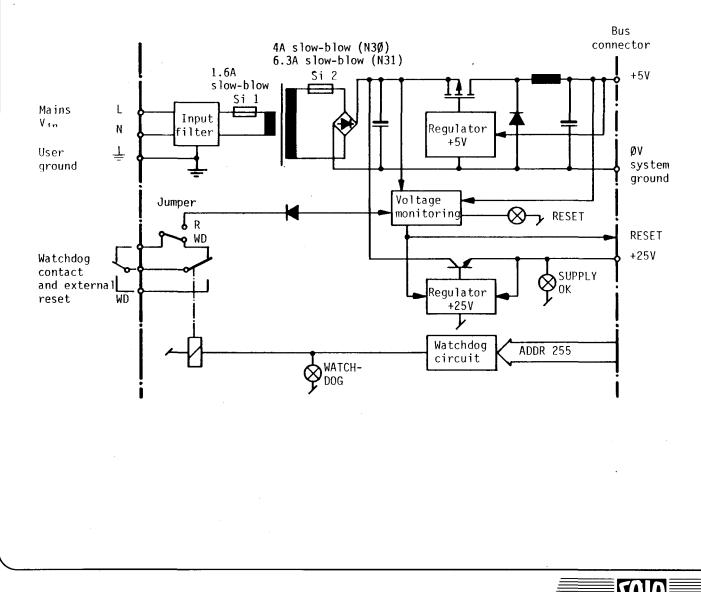
It is recommended to remove all modules (except N3 \emptyset /N31 and the CPU) from the rack when copying EPROMs in the operating mode LCM. Thus, minimal loading of the 25V-voltage is guaranteed.

Modification possibility for a fast external reset

On delivery, the jumper WD/R is inserted in WD. Thus, the reset contact is connected to the connection terminal. The outputs are reset in case of a voltage failure within approximately $5\emptyset - 2\emptyset\emptyset$ ms depending on the modules of the PCA2. If the jumper is inserted in R, a fast external reset can be effected (provided that supply voltage is available). If the voltage potential of \emptyset V is applied to this terminal, all outputs are reset within <u>2ms</u>.

The outputs remain reset for at least 100ms. If a reset signal persists, they remain reset for t + 25ms.

Block circuit diagram



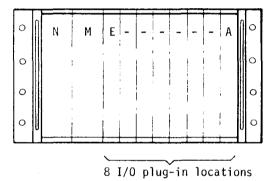
A 7 Type PCA2.C.. Rack units

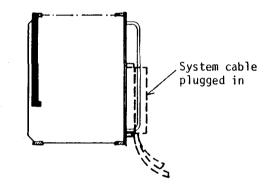
General

All rack units plug in at the rear in the continuous parallel rack bus with the appropriate bus plugs. Therefore, each module can virtually be plugged into any desired location. For reasons of width, the left-hand locations are reserved for the supply and processor modules. Following these, there are locations for 1 to 10 slim modules (all types E, A, W, F and H). Unused locations are covered with plates.

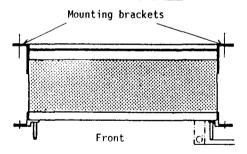
The rack unit has all-round screening. All connections are located on at the front enabling it to be wall-mounted by using the appropriate angle brackets.

A 7.1 Type PCA2.C21 Rack unit with 8 I/O plug-in locations





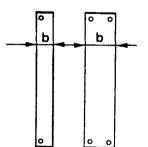
Angle bracket for wall mounting (order no. $4'121'4889'\emptyset$)



Two angle brackets fastened with srews at the rear of the rack unit enabling it to be wallmounted. See dimension diagram.

Coverplates

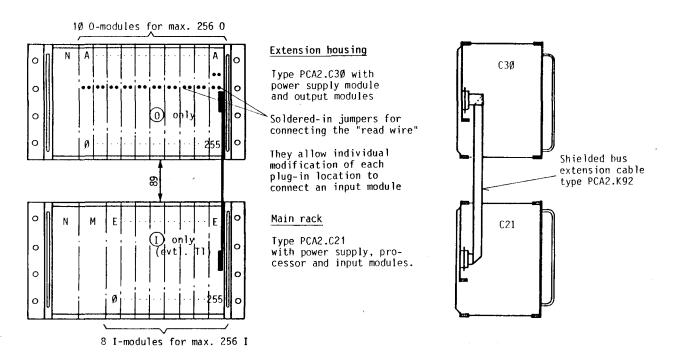
"Slim" version b = 31.4 mm order no. 4'107'4836'0 "Wide" version b = 75.8 mm order no. 4'107'4846'0



A 7.2 Type PCA2.C21 and C3Ø Extension housing for I + 0 > 256

With certain restrictions concerning the software it is possible to increase the capacity to 256 I + 256 O. For this, the extension housing PCA2.C3Ø is required for accomodating output modules. In order to meet the internal power requirements of the additional I and O, another power supply module must be inserted in the extension housing C3Ø.

The C21 is the main housing and has to be connected with the extension housing by the bus extension cable PCA2.K92.



The restrictions regarding the software for the increased no. of I/O are due to the fact that the outputs of the extension housing C3Ø can only be set or reset, their logic states, however, cannot be interrogated. Consequently:

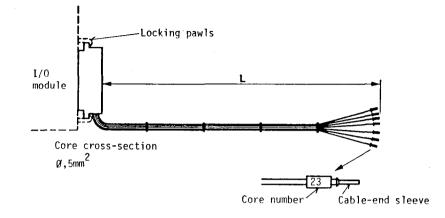
- Inputs and outputs have the same address range \emptyset ...255.
- Inputs can be interrogated in the normal way and linked to other inputs, flag memories, timers or counters.
- <u>Outputs</u>, however, <u>cannot be interrogated</u> or <u>linked directly</u>, i.e. <u>only the</u> following commands are admissible for outputs in this configuration.

OUT, SEO, REO

In order to be able to process logic states of outputs nevertheless, it is recommended to set a flag memory along with such outputs, if necessary (OUT, SEO, REO). The state of these flag memories which is a copy of the respective output can be interrogated and linked at any time.

It is also possible to use only flags in the entire program instead of outputs, as those are not restricted. In the circulating program the used flags are then transferred (in indexed form) to the corresponding outputs. It must be noted, however, that the last mentioned variant results in longer response times for A.

A 8 Type PCA2.K.. System cables

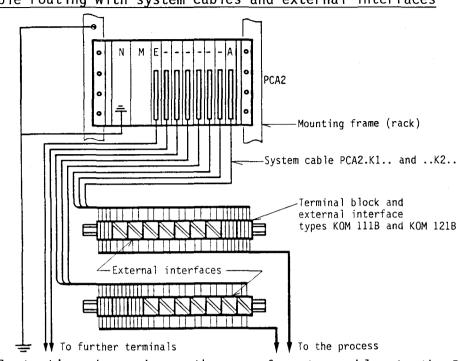


Connection to the front plug of the input and output modules is effected simply and without trouble by using the so-called system cables. This cables are equipped at one end with the module plug with locking device, and, at the other end, with numbered cable-end sleeves. The individual core numbers correspond exactly with the numbers on the pin assignment plans as evident from the relevant I/O documents.

The actual cable is not sheated but comprises the individual cores which are held together by several cable straps at intervals of approximately 20 cm. This provides the necessary flexibility to enable the cable to be routed in all cable ducts. To make the cable flatter, the straps concerned must only be cut carefully.

Two versions having different lengths are available as required:

34 35 34 see module leaflet) 33 33 32 PCA2.K11 length L 1.5m 30 31 30 PCA2.K12 length L 2.5m (standard) 26 27 26 24 25 24 PCA2.K15 length L 5.5m 22 23 22 24 PCA2.K15 length L 5.5m 22 23 22 20 21 20 PCA2.K21 length L 5.5m 18 19 18 0-module PCA2.A4Ø and A31, but als for all other I/O modules 1.5m 14 15 14 PCA2.K21 length L 1.5m 12 13 12 PCA2.K22 length L 1.5m 10 11 10 PCA2.K24 length L 2.5m (standard) 18 9 8 PCA2.K25 length L 1.5m (standard) 12 13 12 PCA2.K24 length L 1.5m (standard) 19 11 6 7 6 8	m s PCA2.K11 1 PCA2.K12 1 PCA2.K12 1 PCA2.K14 1 PCA2.K15 1 PCA2.K25 1 PCA2.K22 1 PCA2.K22 1 PCA2.K25 1 The module	36 34 32 30 28 26 22 22 22 20 18 16 14 12 10 8 6 4	37	36 34 30 28 26 24 22 20 18 16 14 12 10 3 6 4 2 2	٥
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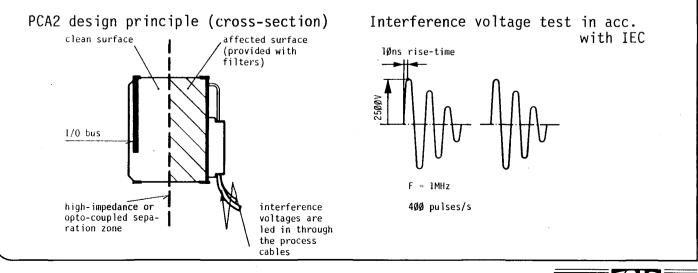


As the illustration above shows, the use of system cables to the PCA2 facilitates the arrangement of the connecting modules to the process in a simple and clear manner. In order to achieve a high degree of interference immunity, the PCA2 must be well grounded via the supply module. The ground connection is distributed to all the modules via the tightly fastened front screws.

A 8.2 Interference immunity

The system cables and also the cables between switch cabinet and process can be routed without problems in the normal cable duct for the contactors, valve and motor cables, as long as the distances do not exceed approximately 50 m. It is recommended that a separate cable duct be used in case of greater distances.

The interference immunity of the I/O modules is tested in accordance with IEC 255-4/E5 class III in order to be able to give reproducible values. This means, that, due to the well-planned circuitry principle of the SAIA°PLC, high voltage peaks (applied directly to the 24V inputs/outputs!) do not interfere with the function and cannot lead to the destruction of components (see figures below):



A 8.1 Cable routing with system cables and external interfaces

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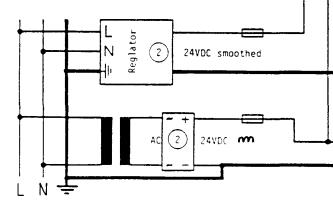
Notes:

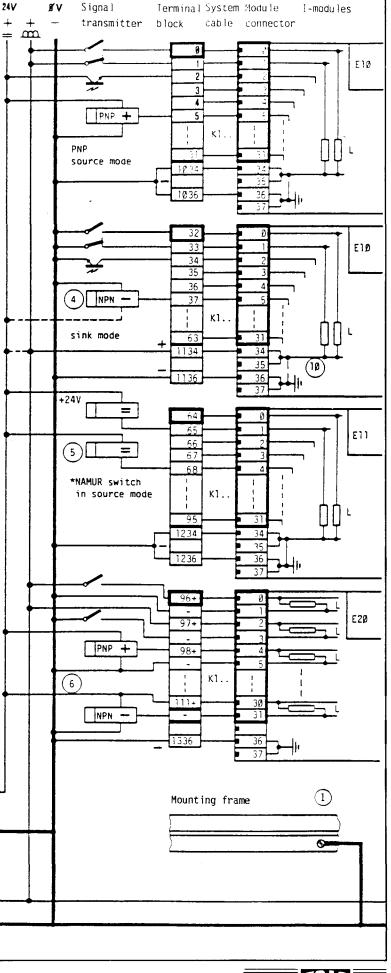
1

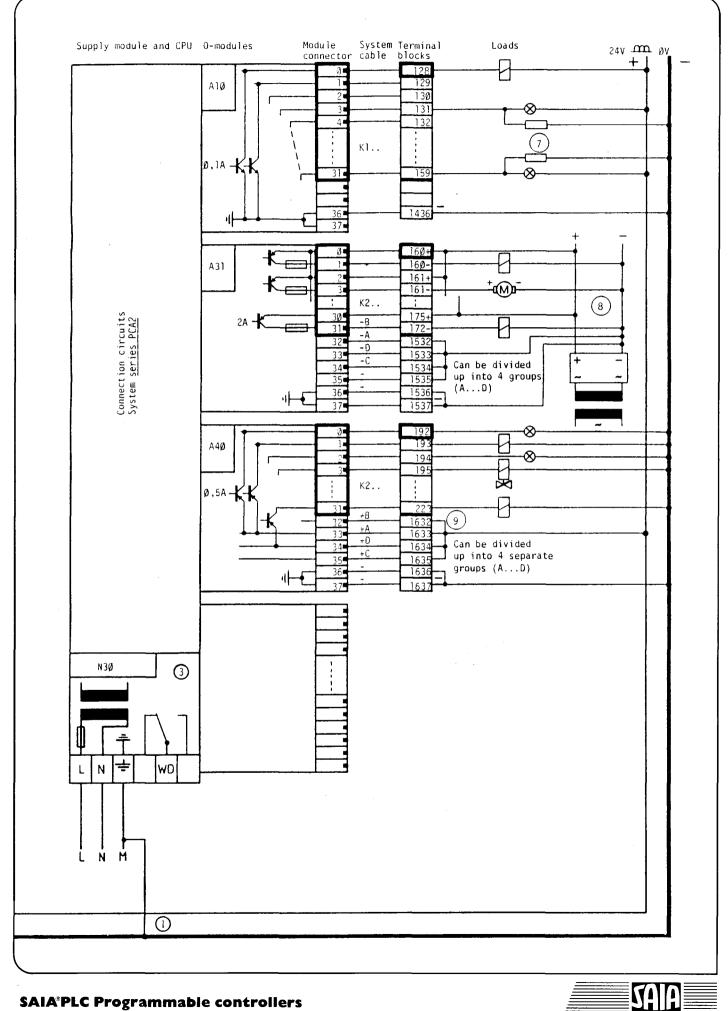
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Circuit information:

- 1 The PLC mounting frame, supply module earth terminals and the negative pole of the 24Vsupply (with the exception of the isolated I/O) are to be connected to a good, common ground. In order to distribute the ground to all modules, their front screws are to be securely tightened.
- 2 The overall 24VDC supply can be a pulsating DC. It is only necessary to have a regulated smoothed voltage, where this is demanded by the transmitter or the load. Proximity switches for example have to some extent close voltage limits and will in most cases only tolerate ripple of up to 10%.
- 3 The power supply module is operative on starting up. The "Fast RESET" function is feasible by reinserting the internal jumper R-WD from WD into R (RESET).
- 4 If in sink mode, the load resistors (L) are connected to a regulated +24V-supply, NPN proximity switches can also be connected here.
- 5 NAMUR proximity switches are connected to NAMUR inputs type E11.*
- 6 With the isolated input circuit type E2Ø independent of the type of connection - the closing of a contact or the driving of a proximity switches can also be connected here. In this event, the supply voltages can be of differing potentials.
- 7 For damping the turn-on current of larger signal lamps, these can be fitted in AlØ with bleeder resistors. With the AlØ module, the positive potential could be different for each load.
- 8 The A31 isolated 0-module can be supplied with a separate circuit. The 16 outputs can be divided into 4 groups on the negative side.
- 9 With the A4Ø 0-module, the 32 outputs on the positive side can be divided into 4 groups.
- 10 In the case of new modules, this bridge must be removed for sink mode.
 - *) Details see PCA2.E1Ø and PCA2.E11, but also the special NAMUR module PCA2.E3Ø.



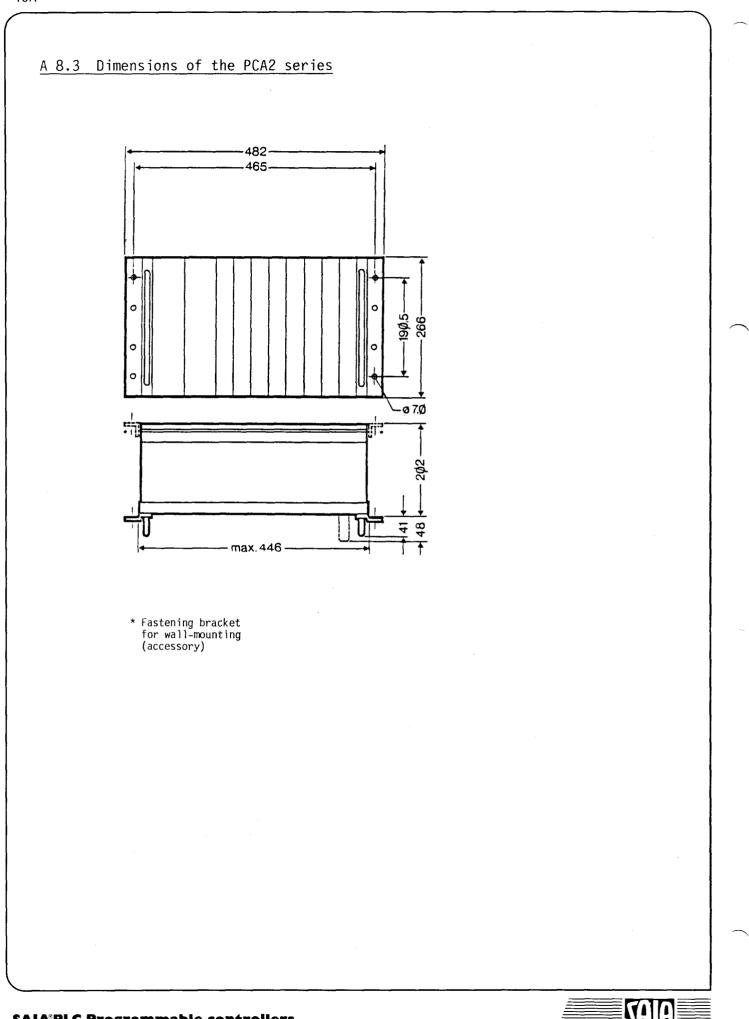




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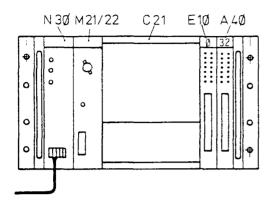


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A 9 Brief instruction for operating a PCA2

a) Equipment



The following modules are plugged into the rack unit from the left to the right:

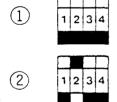
- the power supply module PCA2.N3Ø - the processor module PCA2.M21 (or M22/32)
- the input module PCA2.E1Ø
- the output module PCA2.A4Ø or A1Ø
- the buffered RAM memory module
- R95/R96 is plugged onto socket PROG of the processor module

The large gap between M21 and E1Ø is of advantage, as the storage module can be easily removed at any time.

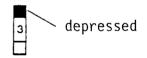
b) Addressing of the I/O

In order to try out the programming examples in manual "Software 1H", it is recommended to select the addresses \emptyset ...31 for the I-module PCA2.E1 \emptyset and 32...63 for the O-module PCA2.A4Ø.

The selection is effected with the DIL-switches by setting the corresponding basic addresses:

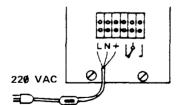


E1Ø-module, basic address Ø



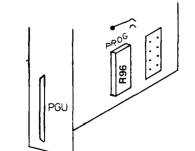
A4Ø-module, basic address 32

c) Power supply



(3) For "playing", it is recommended to provide for a switch in the mains connection in order to reset all resettable elements and the STEP-counter to the defined starting positions at any time by switching off the PCA2.

d) Insertion of the RAM-module and connection to the programming unit PØ5



(4) The buffered RAM-memory module PCA1.R95 or R96 is plugged onto socket "PROG" (groove at the top). The jumper disposed above is inserted in "EPROM" (factory setting). Jumper "WRITE ENABLE" must be inserted (factory setting).

(5) Programming unit PØ5 is connected with connector PGU and secured with the sliding lock.

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- (6) Set operating mode selector switch to "MAN"
- (7) Apply voltage to the power supply module

---> The yellow N3Ø lamp "SUPPLY OK" lights up ---> The yellow M21 lamp "CPU RUN" flashes 1s on, 1s off ---> The PØ5-display lights up

If the operating mode selector switch was set to "MAN", functioning of the I/O-modules can be checked.

- (8) Type in [A] 15 on PØ5. If input 15 is activated, the display in the "operand" changes from Ø to 1 (cannot be checked before connecting the simulating unit S1Ø according to point 18).
- (9) Type in [A] 32 [E] 1 . The LED of output 32 lights up. Upon entering Ø the LED goes out again, i.e. the corresponding output is no longer active.

- f) Programming example "Flashing indicator"
 - (10) Set operating mode selector switch to "PROG".
 - (11) Switch on power supply of the PCA2. The CPU lamp (yellow) flashes 1s on, 1s off.
 - (12) Enter the following indicator program with PØ5.

	STEP	CODE	<u>OPERAND</u>	<u>Program in mnemonic code</u>
A E E E E E E E E	(ØØØØ)* (ØØØ1) (ØØØ2) (ØØØ3) (ØØØ4) (ØØØ5) (ØØØ6)	(ØØ) Ø2 14 ØØ 13 2Ø (ØØ)	(ØØØØ) 256 256 5 32 1 (ØØØØ)	STL 256 STR 256 Ø.5s COO 32 JMP 1

*) The values in brackets are displayed although they do not have to be entered.

(13) Set operating mode selector switch to "RUN". Switch off PCA2 and switch on again.
 ---> Program is being executed, i.e. output 32 flashes Ø.5s on and Ø.5s

off (frequency 1Hz).

- (14) If the time base must be modified to 1/100s, proceed as follows: Switch off PCA2, reinsert jumper (circuit board in the middle, on the left) from 1/10 to 1/100. Switch on PCA2 again. ---> The output 32 flashes 10 times faster, i.e. at a frequency of 10Hz. The selection of the time base 1/100s is also recognized by the increased flashing frequency of the CPU lamp (yellow).
- g) Flashing indicator example with activated watchdog

If in the preceding example the watchdog is to be activated, the instruction COO 255 must be added to this circulating program. In order that this instruction is executed during each cycle independent of the indicator program, enter SEA before.

The supplement is programmed as follows:

(15) Set operating mode selector switch to "PROG".

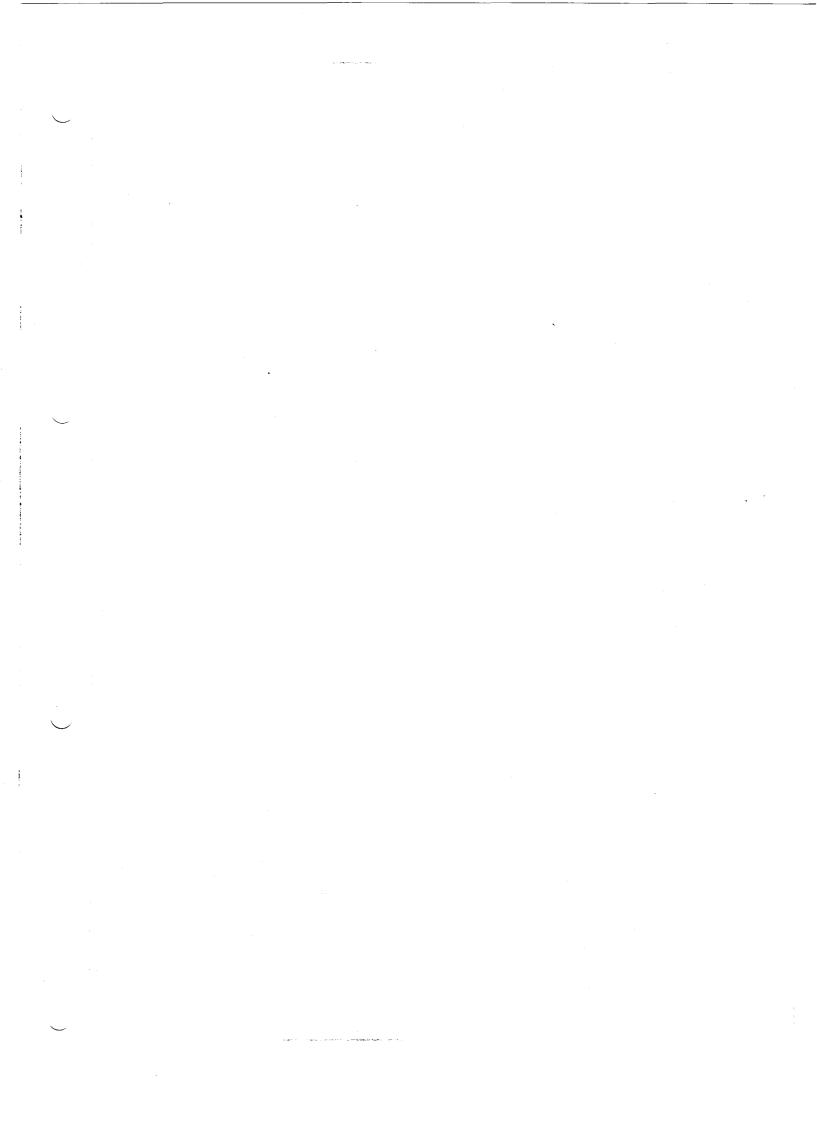
(16) Enter:

				Mnemo	nic code
Α	5	(2Ø)	(1)	4	
Е	(ØØØ5)	19	ø	SEA	ø
Ε	(ØØØ6)	13	255	C00	255
Ε	(ØØØ7)	2Ø	1	└── JMP	1
Е	(ØØØ8)	(ØØ)	(ØØØØ)		

PART B	Input/output modules as well as additional and display modules
Chapter B 1	Plug-in input/output modules
Chapter B 2	Programming units, additional units and accessories

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B 1 Plug-in input/output modules

<u>B 1.1 Digital input modules</u>

- PCA2.E11 32 inputs, for NAMUR proximity switches, electrically connected 24VDC smoothed Input current: Ø...6mA
- PCA2.E2Ø 16 inputs, opto-isolated, each input is independent and potential-free 24VDC smoothed or pulsating Input current: 12mA
- PCA2.E3Ø 32 inputs, for NAMUR-proximity switches, electrically connected 8.4VDC from 24VDC supply voltage Input current: Ø...3.2mA
- PCA2.E6Ø 32 inputs, opto-isolated 24VDC smoothed or pulsating Input current: 10mA

<u>B 1.2 Digital output modules</u>

- PCA2.A1Ø 32 outputs, electrically connected 5...32VDC smoothed or pulsating Output current: 1mA...Ø.1A sink operation
- PCA2.A21 16 outputs with relay contacts, opto-isolated 50VAC/2A, 50VDC/1A, 60VDC/0.8A
- PCA2.A31 16 outputs, opto-isolated 6...36VDC smoothed or pulsating Output current: 5mA...2A, source operation
- PCA2.A4Ø 32 outputs, electrically connected 5...32VDC, smoothed or pulsating Output current 5mA...Ø.5A, source operation

B 1.3 Analog input/output modules

Analog input/output module PCA2.W1

12-bit resolution

PCA2.W1Ø	- 8 input channels (without output)
PCA2.W12	- 8 input channels, 2 output channels
PCA2.W14	- 8 input channels, 4 output channels
PCA2.W15	- (without input), 4 output channels
PCA2.W16	- 8 input channels, (without output)

Analog input modules PCA2.W2

8-bit resolution

PCA2.W2Ø PCA2.W21			input channels Ø1ØV Stand input channels Ø5V	lard
PCA2.W22 PCA2.W25 PCA2.W26		16 32 32	input channels Ø2ØmA input channels Ø1ØV Stanc input channels Ø5V	lard
PCA2.W27	-	32	input channels Ø2ØmA	

B 1.4 Counter module for 10...200kHz

PCA2.H1 - Counter module PCA2.H11 - Additional counting mode module PCA2.H12/13 - Additional stepping motor module

<u>B 1.5 Data line switching module</u>

PCA2.F2Ø - For 4 serial interfaces RS 232c or current loop 20mA



2B

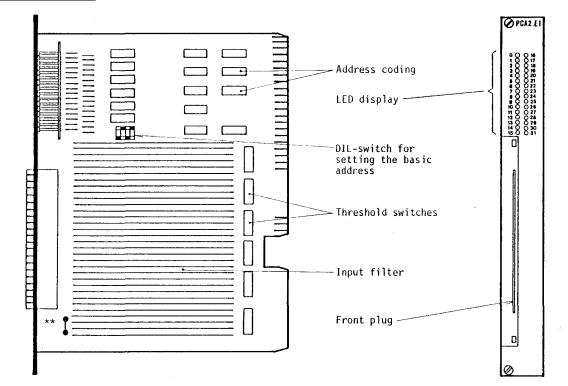
<u>B 1.1 Digital input modules</u>

B 1.1.1 Type PCA2.E1Ø Input module, electrically connected

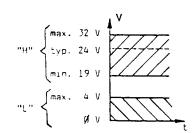
<u>Technical data</u>

Number of inputs per module	32, electrically connected
Input voltage Vin	24VDC smoothed or pulsating
Input current at 24VDC	1ØmA
Typical input delay	8ms

Presentation



Definition of input voltages



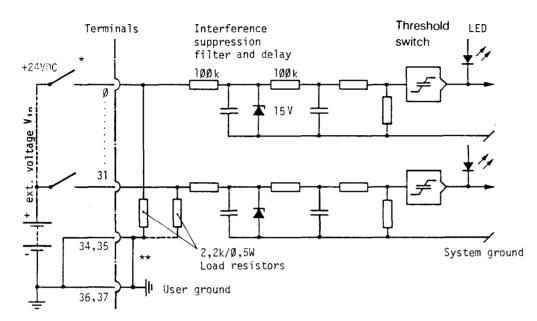
On account of the 8ms input delay pulsating DC-voltage is sufficient for external supply.

*) This jumper must be removed in sink operation.

Input circuit

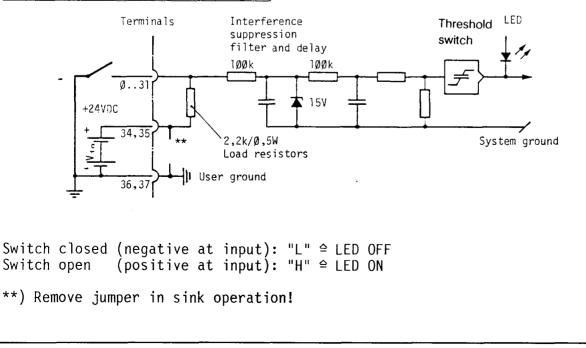
Depending on the external circuitry, this module can be used in source or sink operation.

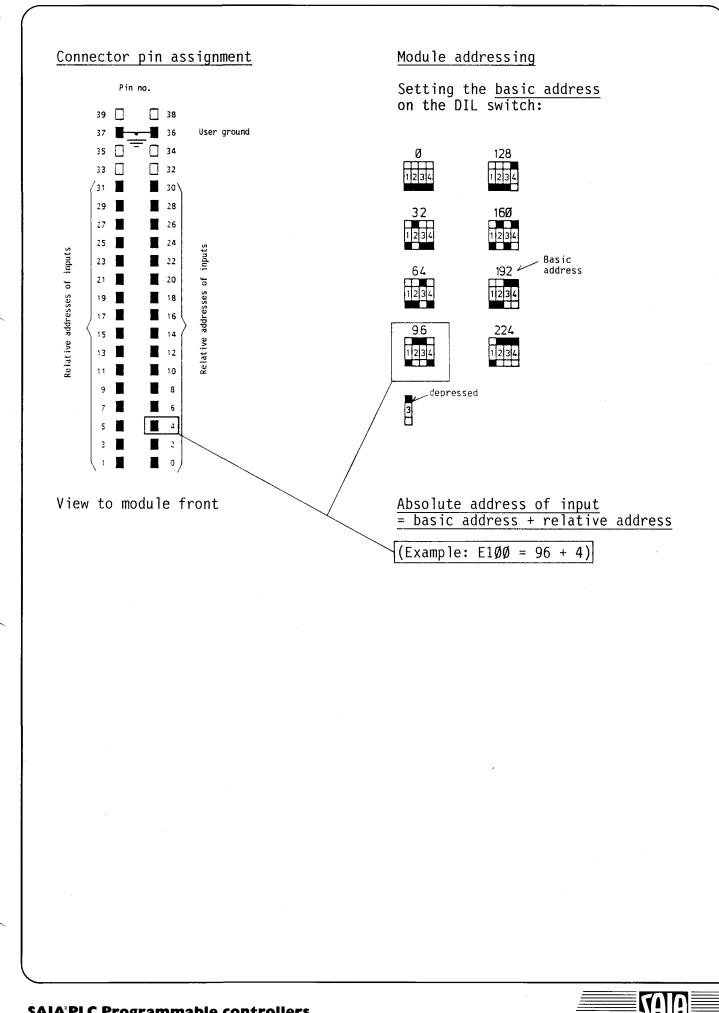
Source operation or positive logic (normal case):



*) PCA2.E1Ø is also suitable for NAMUR switches which can carry a current of 10mA at 24VDC and 2.2k Ω .

Sink operation or negative logic:





B 1.1.2 Type PCA2.E11 Input module for NAMUR proximity switches

Due to the object distance, NAMUR proximity switches supply a current from \emptyset to 6mA. To give consideration for these special conditions, two resistors are changed per input in the NAMUR version as opposed to the standard PCA2.E1 \emptyset card.

Technical data

Number of inputs per module

32, electrically connected

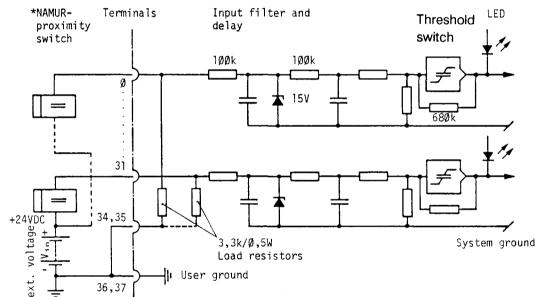
Voltage source $V_{\mbox{\scriptsize in}}$ in series with NAMUR proximity switches

24VDC smoothed

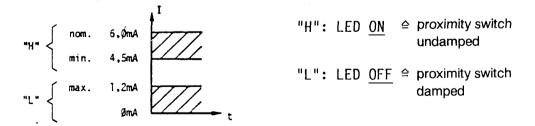
8ms

Typical input delay





Definition of the input variables



See PCA2.E1Ø for connector pin assignment and module addressing.

*) PCA2.E11 is suitable for NAMUR proximity switches which can carry a current of 6mA at 24VDC and $3.3k\Omega$. Type PCA2.E3Ø is a special NAMUR-input module.

B 1.1.3 Type PCA2.E2Ø Input module opto-isolated

<u>Technical data</u>

Number of inputs per module

16, opto-isolated (between process, CPU and each other)

Input voltage V_{in}

24VDC, smoothed or pulsating, each input is independent and potential-free

Input current at 24VDC

Typical input delay

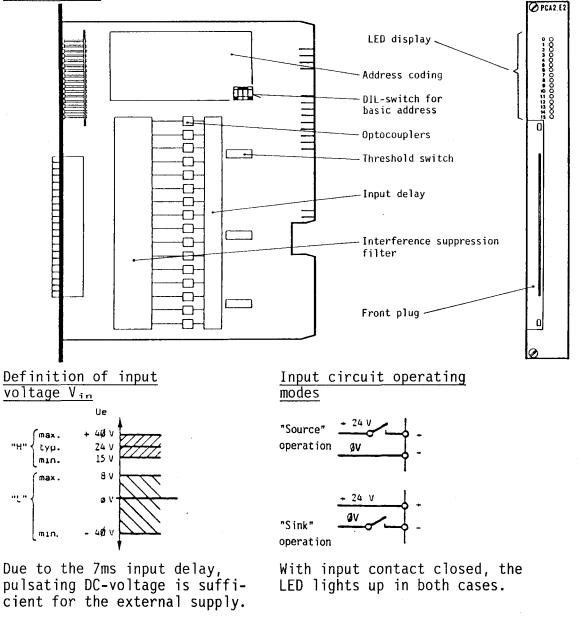
7ms

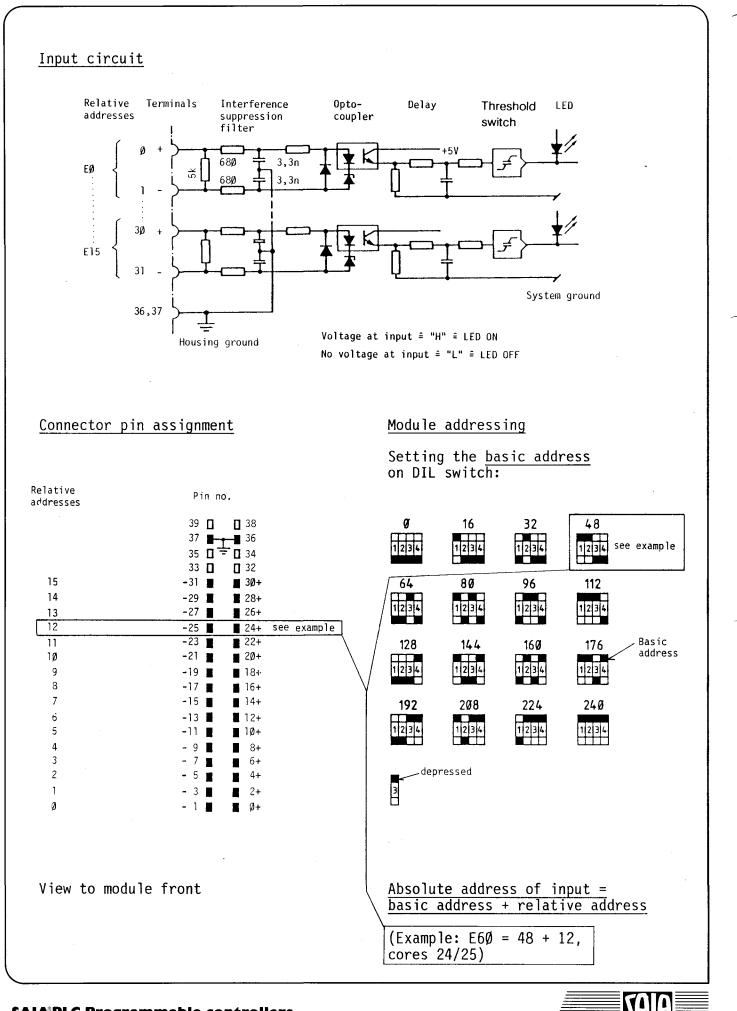
12mA

Isolation voltage of optocoupler

min. 2000V

Presentation





8B

B 1.1.4 Type PCA2.E3Ø Input module for NAMUR proximity switches

Proximity switches according to DIN standard 19234 resp. NAMUR* are simple inductive DC-voltage switches using 2-wire technology. Their power consumption varies depending on the object distance.

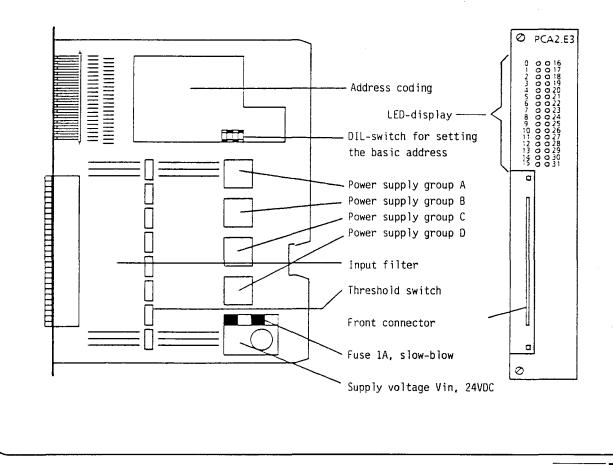
The input module PCA2.E3Ø corresponds to the standard as regards idling voltage, short-circuit current and switching points. However, line break and short-circuit monitoring of the line are not provided.

Technical data

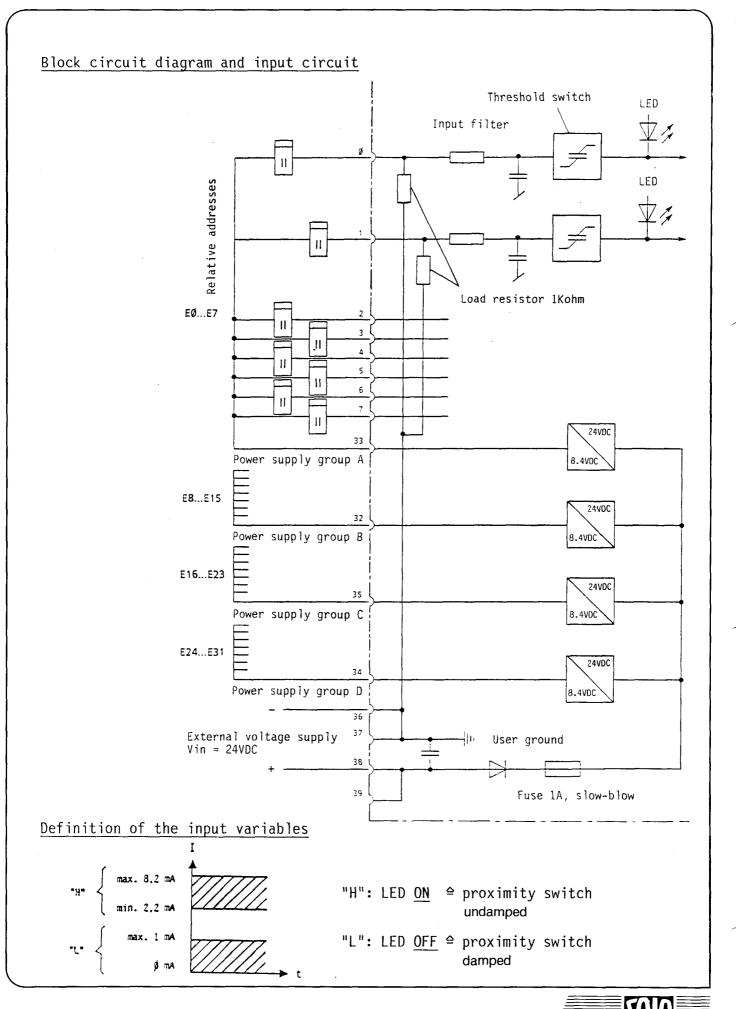
Number of inputs per module	32, electrically connected
Power supply for NAMUR proximity switches	4 groups of 8 switches $V_o = 8.4$ VDC (per module)
External supply voltage V _{in}	24VDC, smoothed or pulsating $\pm 20\%$
Typical input delay	2 ms
Short-circuit current	8.4 mA

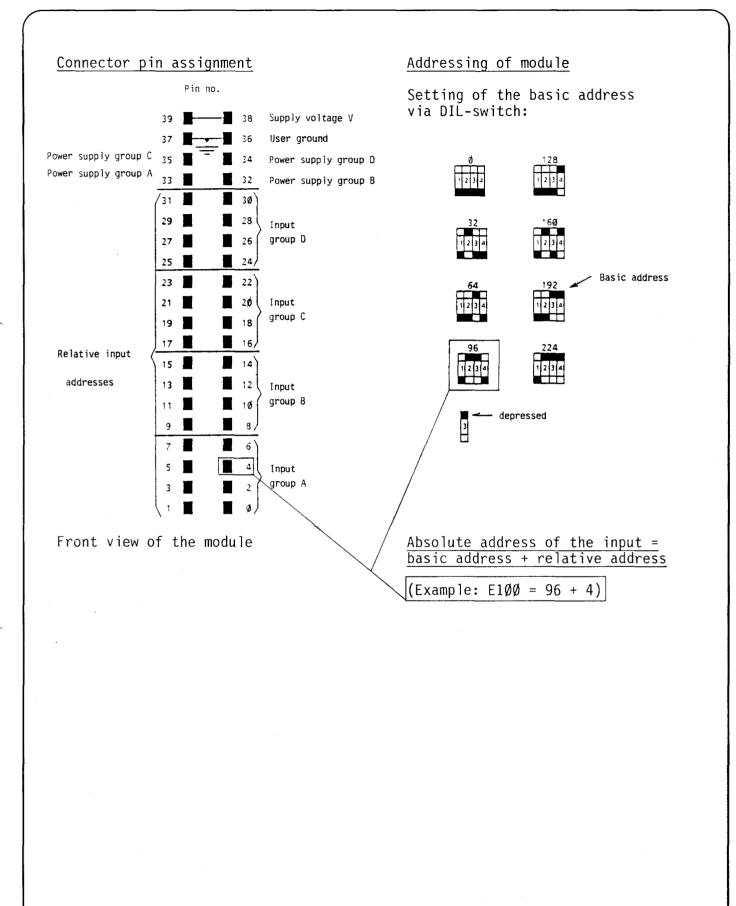
*) NAMUR = Normen-Arbeitsgemeinschaft Mess- und Regeltechnik (Committee for measuring and control engineering standards)

Presentation



9B

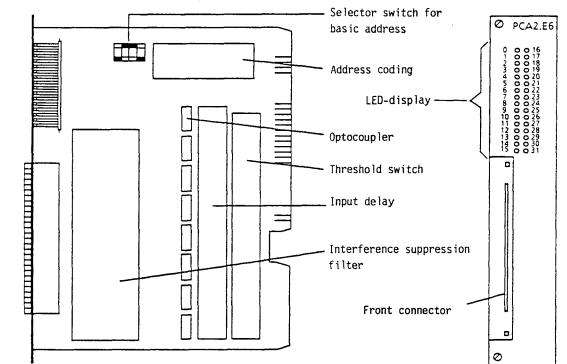




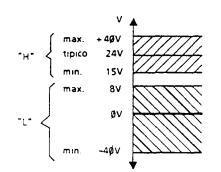
<u>B 1.1.5 Type PCA2.E6Ø Input module opto-isolated</u>

Technical data	
Number of inputs per module	32, opto-isolated (between process and CPU)
Input voltage V _{in}	24VDC smoothed or pulsating
Typical input current at 24VDC	1ØmA
Typical input delay	7ms
Isolation voltage of optocouplers	AC 5ØØØV eff.

Presentation

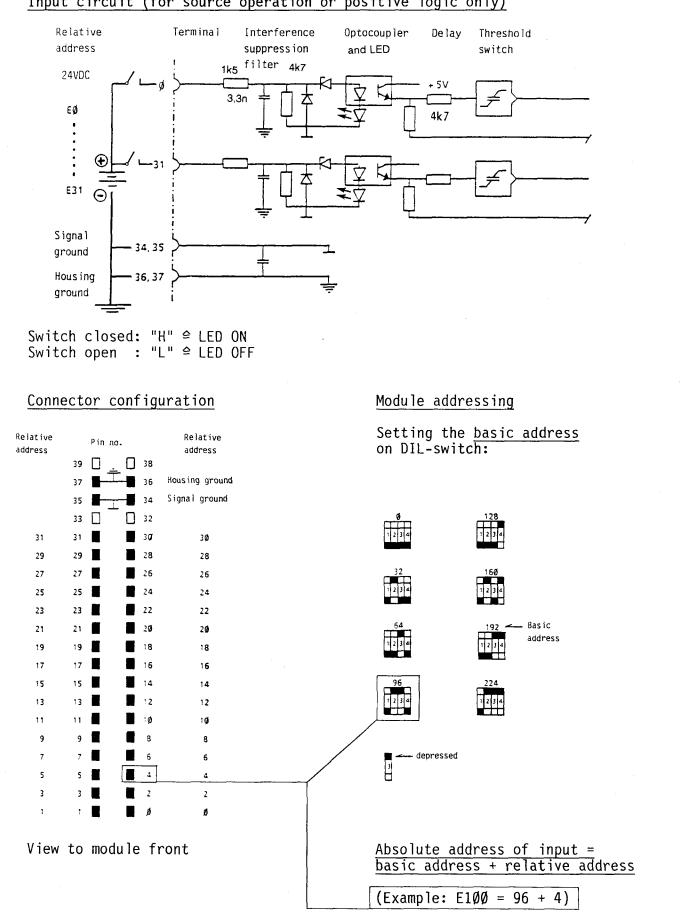


Definition of input voltage Vin



Due to the 7 ms input delay, pulsating DC-voltage is sufficient for the external supply.

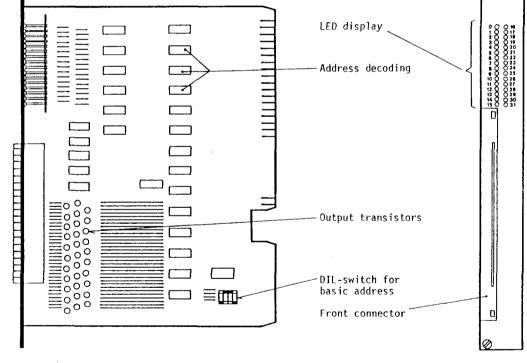
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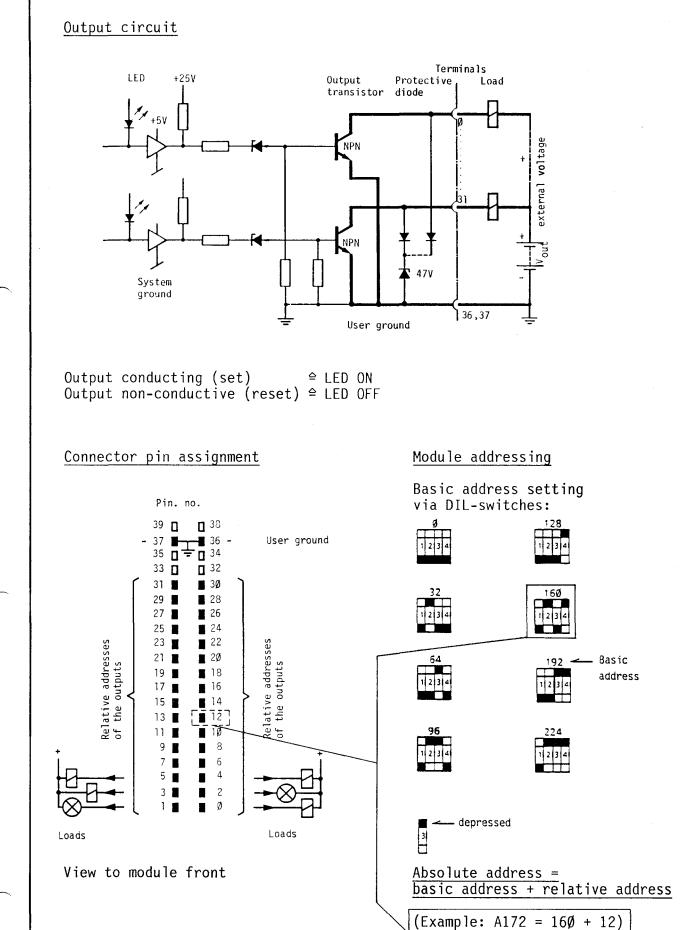
Input circuit (for source operation or positive logic only)

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<u>B 1.2.1 Type PCA2.A1Ø Output modu</u> (sink opera	tion, i.e. <u>negative switching</u>)
<u>Technical data</u>	
Number of outputs per module	32, electrically connected
Output current range	1mAØ.1A In the voltage range 524VDC the load resistance must be at least 24ØΩ
Operating mode	Sink operation (negative switching)
Voltage range Vout	532VDC smoothed or pulsating
Voltage drop	1V at Ø.1A
Typical output delay	10µs (ohmic load)
Presentation	
1	O PCA2.A1



Note: Interference immunity of this negative switching output module is below the 2500V laid down in A 8.2. Therefore module PCA2.A10 should only be used where its specific characteristics are required. In all other cases, the more robust modules PCA2.A31 and A40 are to be employed.



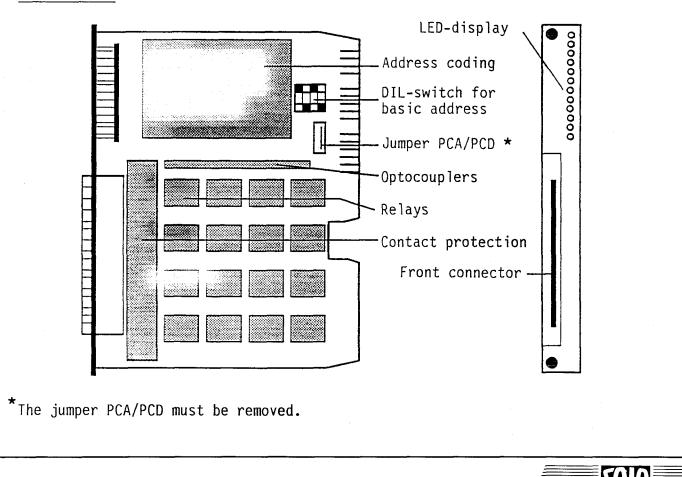
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1

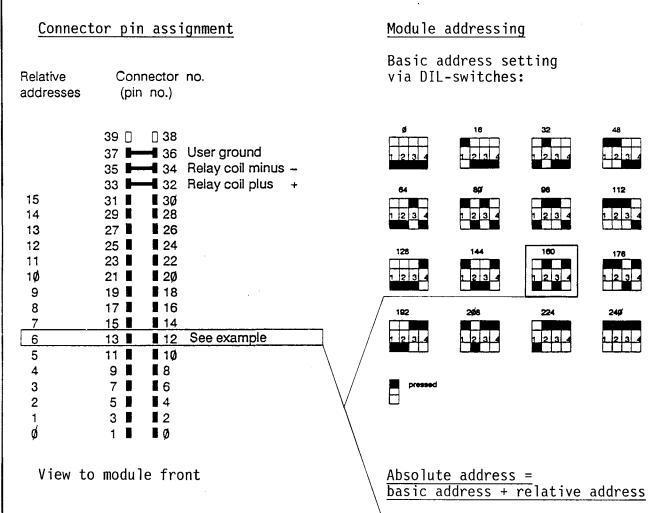
B 1.2.2 Type PCA2.A21 Output module with relay contacts

Technical data Number of outputs per module 16, galvanically isolated, normally open contacts 2A, 5ØVAC Nominal power rating Ø.8A, 6ØVDC *) 1A, 5ØVDC *) (resistive load, inductive load with additional spark suppression) Minimum power rating 1ØmA, 15V Contact life (resistive load 2A, 5ØVAC : Ø.6 mio switching cycles Ø.8A, 6ØVDC: 4 mio switching cycles and 1 switching cycle/s) Relay coil supply 24VDC ±15% IEC 255.4 class 3 and 801.4 class 3 Interference protection *) It is recommended to use transistor outputs when connecting DC-voltages, in order to ensure reliable switching.

Note: To achieve maximum interference protection, position the module PCA2.A21 as far away from CPU and I/O-cards as possible.



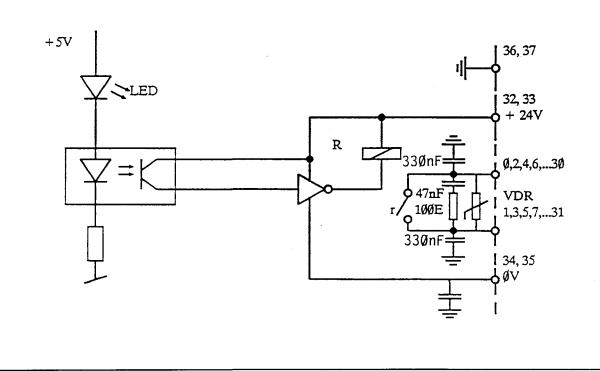
Presentation



(Example: A166 = 16Ø + 6 = core no. 12/13)

TAA

Output circuit





B 1.2.3 Type PCA2.A31 Output module, opto-isolated for 2A

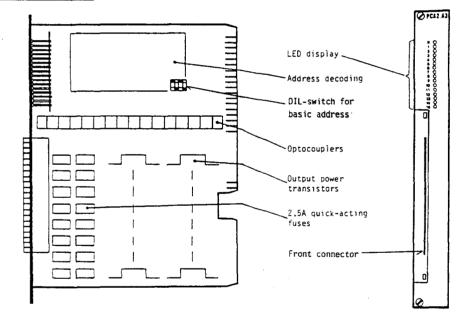
Technical data

Number of outputs per module

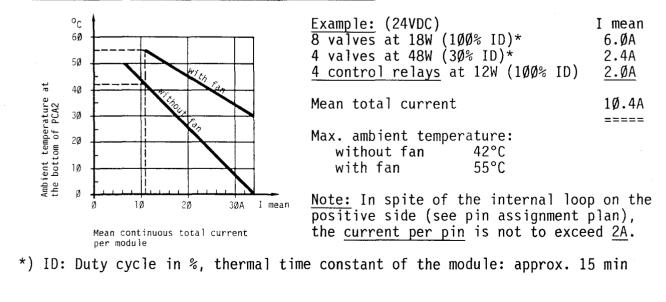
Output current range

16 (subdivided into 4 groups), opto-isolated (between process and CPU) 5mA...2A In the voltage range 6...24V the load resistance must be at least 12 Ω. Source operation (positive switching) 2.5A quick-acting fuse 6...36VDC ≤ 1.5V bei 2A min. 2000V 500μs (i.e. approx. 7 cycles at 70μs)

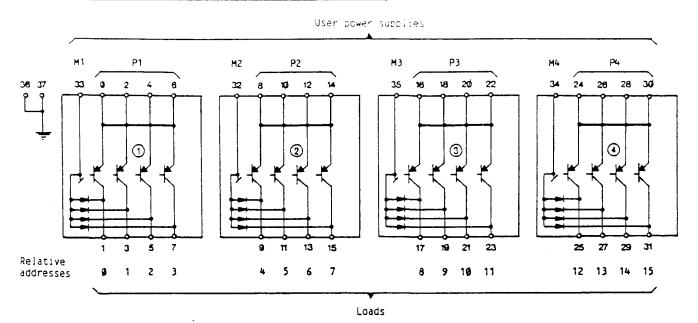
Presentation



Maximum permissible total current per module



Division of the galvanically isolated groups

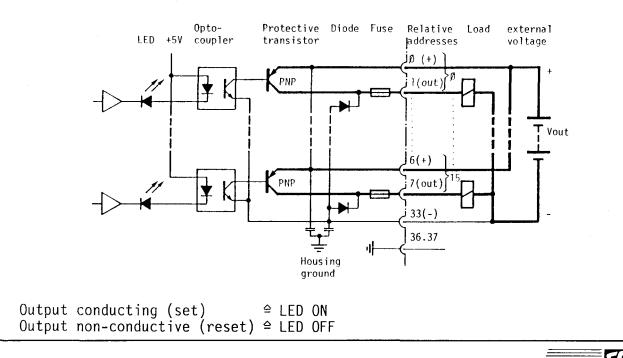


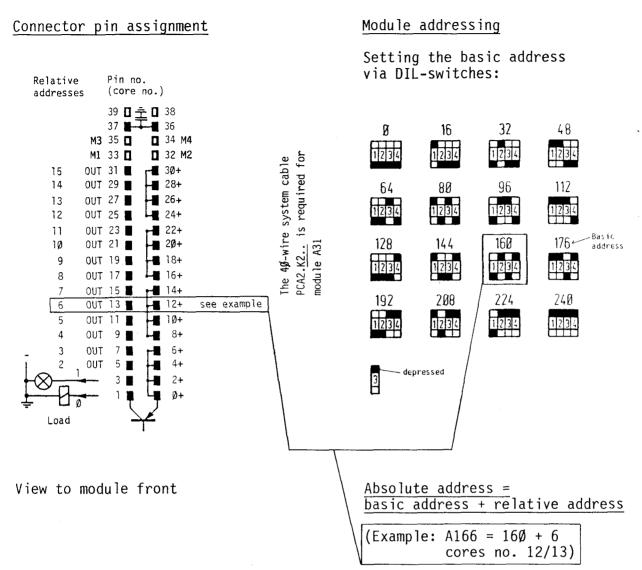
M1, M2, M3, M4: Ground and negative lines of user power supply (1), (2), (3), (4) P1, P2, P3, P4: Positive line of user power supply (1), (2), (3), (4)

The output groups are galvanically isolated from each other and from the CPU. Each group can therefore be supplied with different voltages ranging from 6 to 36VDC. It is of course also possible to connect several or all groups to the same voltage source, provided that they can be protected in accordance with the current intensity of the total current.

The $4\emptyset$ -wire system cable PCA2.K2.. is required owing to subdivision of the output module into 4 groups.

<u>Output circuit of group (1)</u>





5

20B



B 1.2.4 Type PCA2.A4Ø Output module, electrically connected for Ø.5A

<u>Technical data</u>

Number of outputs per module

Output current range

32 (4 x 8) electrically connected 5mA...Ø.5A In the voltage range 5...24VDC, the load resistance must be at least 48 Ω .

Source operation (positive switching)

Total current per module

Voltage range Vout

Operating mode

Voltage drop

Typical output delay

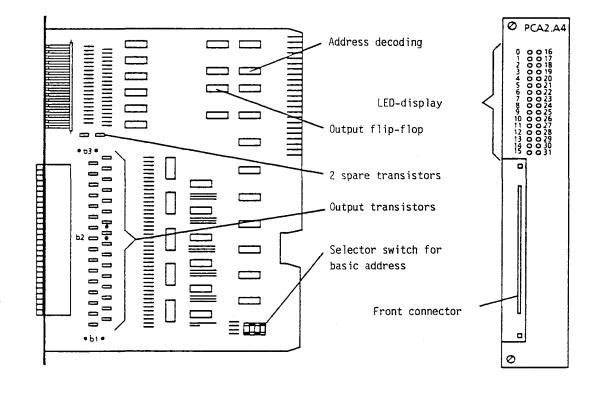
1V at Ø.5A

See drawing

 $10\mu s$ (greater with an inductive load due to free-wheeling diode)

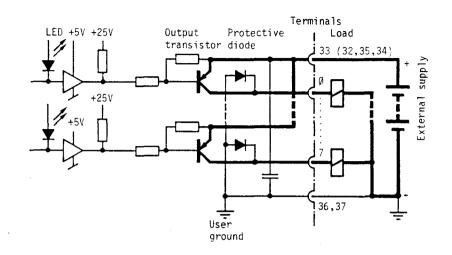
5...32VDC smoothed or pulsating

Presentation



b: Soldering points for locating the positive jumpers (see following page)

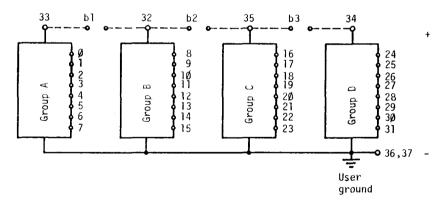




Division of the output groups

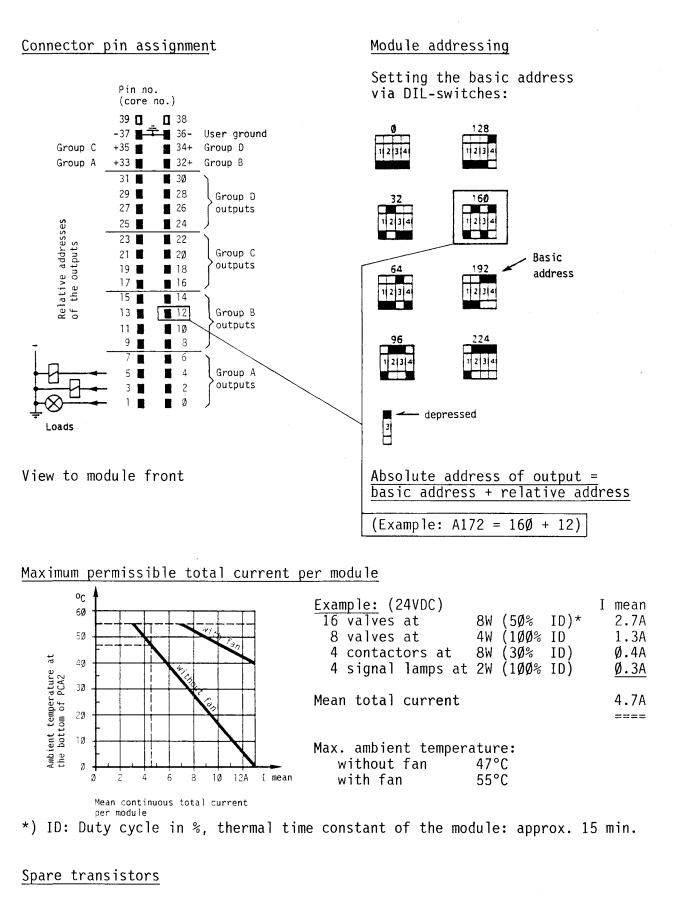
The outputs are non-isolated and have a <u>common ground</u>, which is connected to the <u>negative</u> of the user circuits (pins 36 and 37).

The division of the outputs into 4 groups (A to D) enable however, up to 4 different user supplies to be connected, which have a common negative, the positive voltages, however, can vary over a range of 5...32VDC.



The division of the output module into 4 groups requires the use of the PCA2.K2.. $4\emptyset$ -core system cable.

If the total output current of 4A per module is <u>not exceeded</u> and only one supply voltage is applied, it is possible by soldering in the 3 jumpers (b1 - b3) to use the system cable type PCA2.K1..



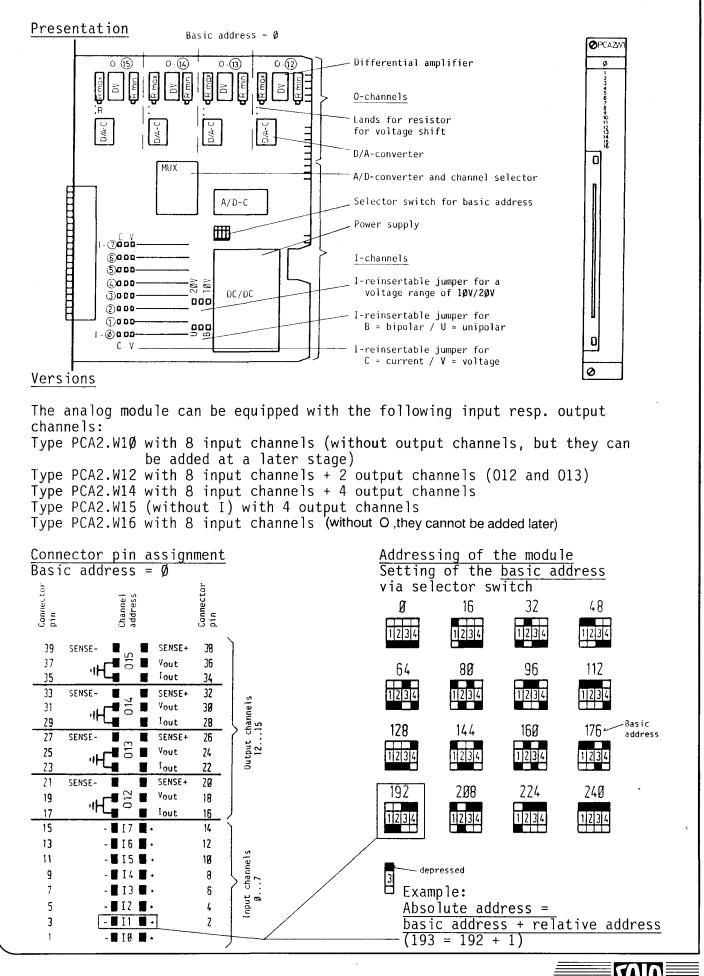
The outputs of module PCA2.A4Ø are not safeguarded. In case an output transistor should become faulty and the user has the necessary skill with a soldering iron, two spare transistors are available on the printed circuit board.

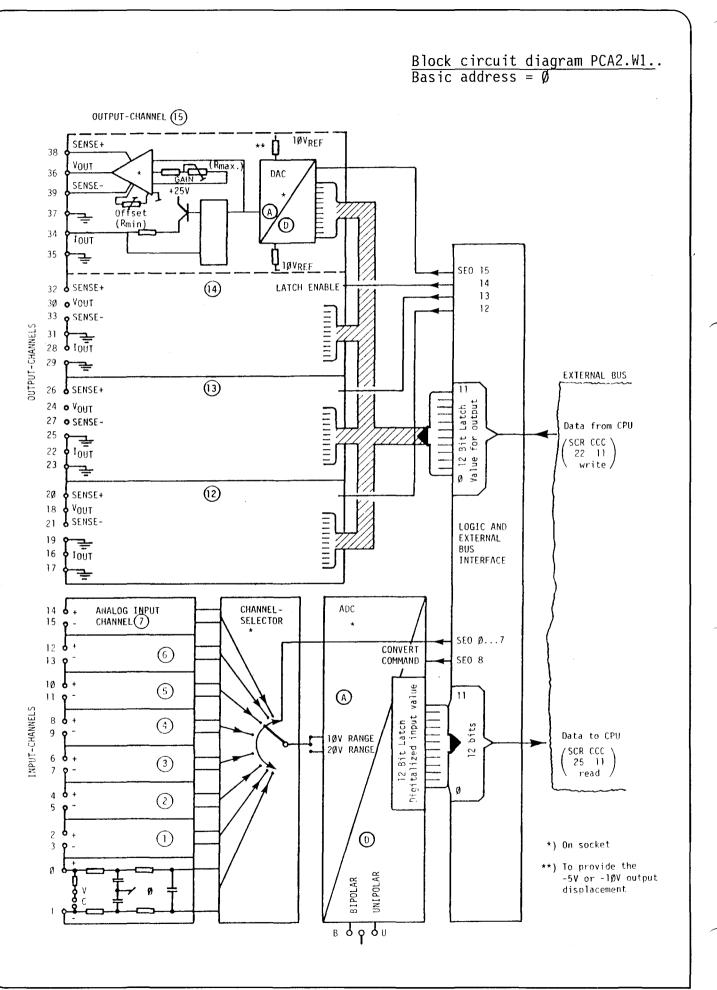
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B 1.3.1 Typ PCA2.W1 Analogo	e Ein- und Ausgangsmodule 12 Bit
<u>Technische Daten</u>	
Eingänge:	
Anzahl Eingangskanäle Eingangsschaltung Signalbereiche: – Spannung	8 bzw. Ø Differential mit Filter 1) ØV+1ØV oder -1ØV ØV durch Stecker 2) -5V +5V +5V5V pro Modul 3) -1ØV+1ØV +1ØV1ØV wählbar
- Strom	<pre>1) Ø+2ØmA 2) -1Ø+1ØmA 3) -2Ø+2ØmA </pre> alternativ als Stromschleife steckbar. Strombereich ent- sprechend dem oben gewählten Spannungsbereich
Auflösung Genauigkeit (absolute Abweichung) Eingangs-Impedanz Zeitkonstante des Eingangs- filters A/D-Umwandlungszeit Ueberspannung	12 Bit = 1/4Ø96 typ. Ø,1% ± 1 LSB*; (max. Ø,5% ± 1 LSB bei Bipolar-Betrieb) ≥ 1MΩ Ø,1ms ≤ 3Øμs geschützt 6ØVDC / Spitzen 2ØØV
Ausgänge:	
Anzahl der Ausgangskanäle Auflösung D/A-Umwandlungszeit Signalbereiche - Spannung	max. 4 12 Bit = 1/4Ø96 ≤ 2Ø μs ØV+1ØV ** standard -5V +5V ∫ spezial (mit individuellen
Genauigkeit Ausgangs-Spannungsvermögen Lastimpedanz	-1ØV ØV J Abgleichwiderständen) typ. Ø,1% ± 1 LSB, max. Ø,3% ± 1 LSB max. + 1Ø,5V inklusiv Kompensationsspannung ≥ 3kΩ
- Strom Genauigkeit Lastimpedanz	Ø+2ØmA (nur positiv) typ. Ø,4% ± 1 LSB, max. 1% ± 1 LSB Ø55ØΩ (Spannungsvermögen max. 11V)

*) LSB: Least Significant Bit; z.B. 1/4096 von 10V: ca. 2,5mV

**) Zwei Messleitungen kontrollieren bei jedem Kanal die tatsächlich am Lastwiderstand empfangene Spannung (der Spannungsabfall auf der Signalleitung sowie kleine Potentialunterschiede zwischen PLC-Anwendermasse und der Masse am Empfangsort werden dadurch kompensiert).





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Software

The operands mentioned in the following examples refer to the basic address \emptyset . The user will convert it according to his application.

Read in analog value

Two steps are necessary: - select input channel - trigger the actual A/D-conversion

The binary value $(\emptyset \dots 4\emptyset 95)$ is now available and can easily be transferred to the counter register by means of the instruction set 1H.

Example::

SEO Ø7*	; Select input channel (Ø7)
SEO 8*	; Trigger A/D-conversion
•	; The digital value is available in the address range Ø (MSB) to 11 (LSB)
SCR 256	; Load this value into counter 256
25 11*	; 12 bit binary

Output analog value

The binary value (\emptyset ...4 \emptyset 95) to be output must be available at the inputs of the D/A-converter.

The desired output channel is then selected and the corresponding analog value output. It remains stored until a new command follows.

Example:

	counter 256 contains the value
	to be output (Ø4Ø95)
SCR 256	supply counter contents of 12 bit
22 11*	to all D/A-converters (Ø:MSB to 11:LSB)
	in binary form
SEO 1215*	select output channel (1215). The binary
	value is stored and converted into an analog
	value in the respective D/A-converter.

Remark

When selecting an input channel SEO \emptyset ...8 also the value being available at the inputs of the D/A-converter will be changed; this does not have a negative effect, however, since no storage command (SEO 12...15) follows.

*) The basic address selected must be added to these operands.



Connection to the process

Connection of the input channels

The common-mode voltage range of all input channels is $\pm 10\%$, i.e., both potentials of each input channel must be within $\pm 10\%$ with respect to the ground in order to allow correct acquisition of the measured data.

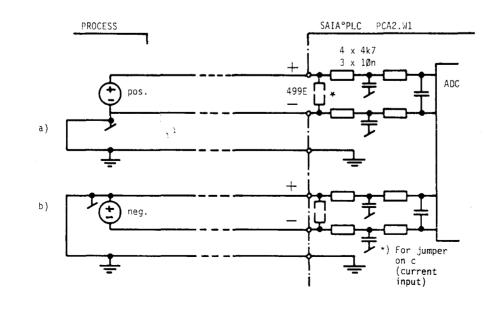
Preselection of the I-ranges:

- <u>The process ground resp. measuring amplifier ground must be connected to</u> the user ground of the PLC.
- The input voltage range of 10/20V is preselected jointly for all inputs of a module via the connector.
- Whether <u>bipolar voltages</u> (±V) or <u>unipolar voltages</u> are to be registered, is preselected jointly for all inputs of a module via the connector B/U.
- <u>Operation with current</u> can be selected for each input individually via the connector (C = current, V = voltage). If the connector is in position C, a precision resistance of 499Ω is connected to this input circuit, the voltage of which is evaluated. The current range depends on the selected voltage range ($10V \simeq 20$ mA).

The following table shows the three basic ranges with respect to the corresponding binary value:

Binary value	Unipolar (U) operation	Bipolar operation (B)	
Value	(connector 1ØV)	(connector 1ØV)	(connector 2ØV)
4Ø95 2Ø48 Ø	+1ØV (+2ØmA) +5V (+1ØmA) ØV (ØmA)	+5V (+1ØmA) ØV (ØmA) -5V (-1ØmA)	+1ØV (+2ØmA) ØV (ØmA) -1ØV (-2ØmA)

<u>In case of unipolar operation</u> the positive potential is applied to the plusterminal. Figures a and b show the connection scheme for the measurement of positive or negative voltages respectively.



Output channels

Apart from the number of output channels $(\emptyset...4)$ it can also be determined whether it is a current or a voltage output. The ranges of the voltage outputs can also be selected individually.

- For a current output, a D/A converter must be on its socket. The current generator on the pc-board is standard. The current range is \emptyset ...+2 \emptyset mA.
- For a <u>voltage output</u> the respective differential amplifier must be inserted in addition to the D/A converter. The current output is also available. According to the following table, the voltage can be changed by using stable resistors.

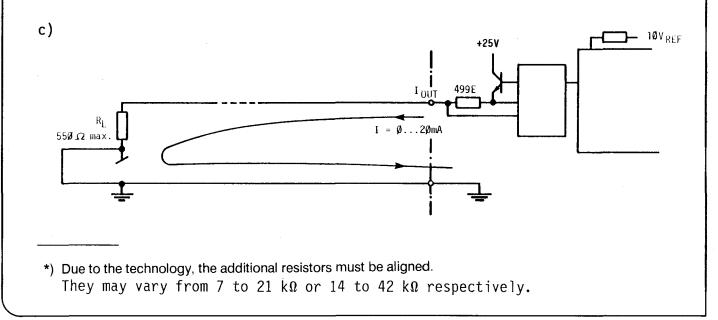
The following table contains a summary of the analog output values and the corresponding binary value.

Binary value	Current output	Standard	Voltage out with resistor* approx. 2ØkΩ	
4Ø95	+2ØmA	+1ØV	+5V	ØV
2Ø48	+1ØmA	+5V	ØV	-5V
Ø	ØmA	ØV	-5V	-1ØV

<u>Connection as current output (figure c):</u>

The current output consists of the D/A-converter and a unipolar power source with high impedance. The voltage of the latter is 11V at 20mA. This corresponds to an external circuit resistance of 0 to 550Ω .

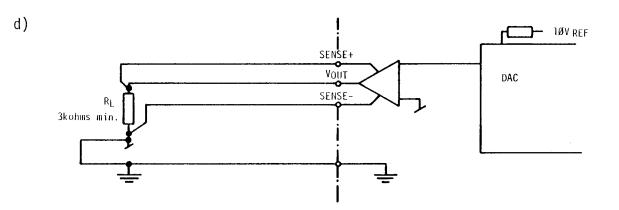
The generated current leaves the PLC with the potential I-out, passes the load and returns to the PLC via the connection process ground - user ground of the PLC. The current does not depend on the external circuit resistance (up to $55\emptyset\Omega$) and minor differences in potential of both grounds.



Connection as voltage output (figure d):

The voltage output consists of the pluggable D/A-converter and the differential amplifier which is also pluggable.

In order to increase the accuracy of the voltage at the load, the two potentials "sense +" and "sense -" are applied. This measuring circuit has a high impedance ($I \leq 3\mu A$). Wiring according to figure d) has the result that a voltage loss in the circuit V-out and minor differences in potential between the process ground and the PLC-ground is automatically compensated for (output voltage = 10.5V).



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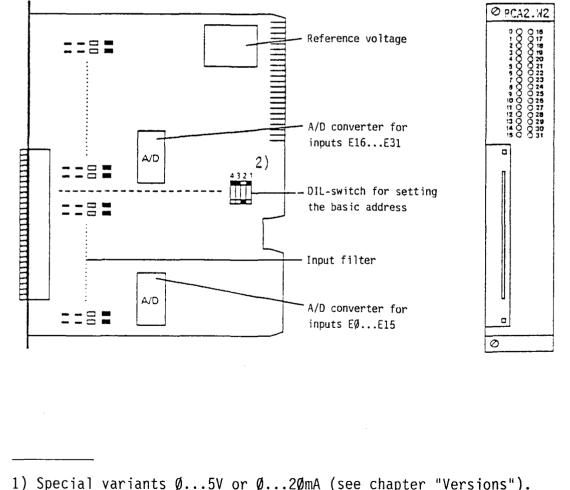


B 1.3.2 Type PCA2.W2.. Analog input module with 8-bit resolution

Technical data

Number of input channels	16 or 32
Voltage range	Ø1ØV 1)
Resolution	8 bits (1/256 ≙ Ø.4%)
Accuracy	1 1/2 Bit ≙ Ø.6%
Static input impedance	\geq 1MQ
Time constant of the I-filter	Ø.2ms
A/D-conversion time	< 100µs
Current consumption	5V: 36mA, 25V: 4mA (average)

Presentation



Special variants Ø...5V or Ø...2ØmA (see chapter "Versions").
 The on/off setting on the DIL-switch is reversed in comparison to usual modules.

<u> (al</u>i)

Versions

Two standard versions are available:

Type PCA2.W2Ø with 16 I-channels, Ø...1ØV Type PCA2.W25 with 32 I-channels, Ø...1ØV

```
Special versions (available on request)
```

Type PCA2.W21 with 16 I-channels, Ø...5V Type PCA2.W22 with 16 I-channels, Ø...2ØmA Type PCA2.W26 with 32 I-channels, Ø...5V

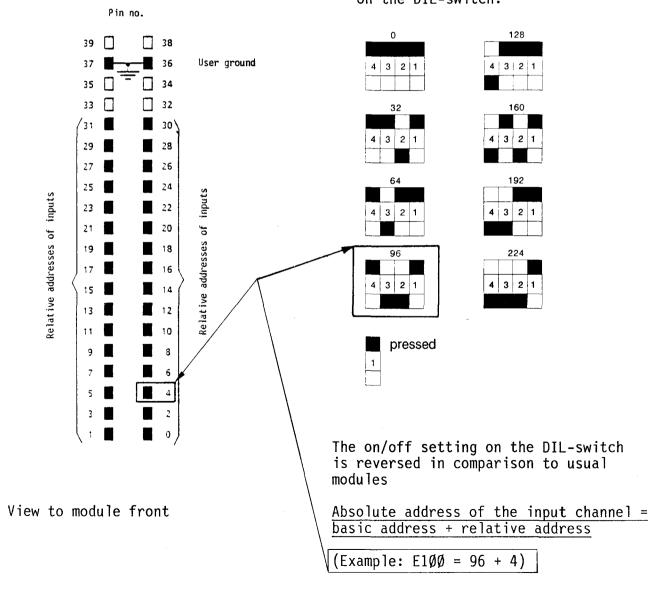
Type PCA2.W27 with 32 I-channels, Ø...20mA

Connector pin assignment

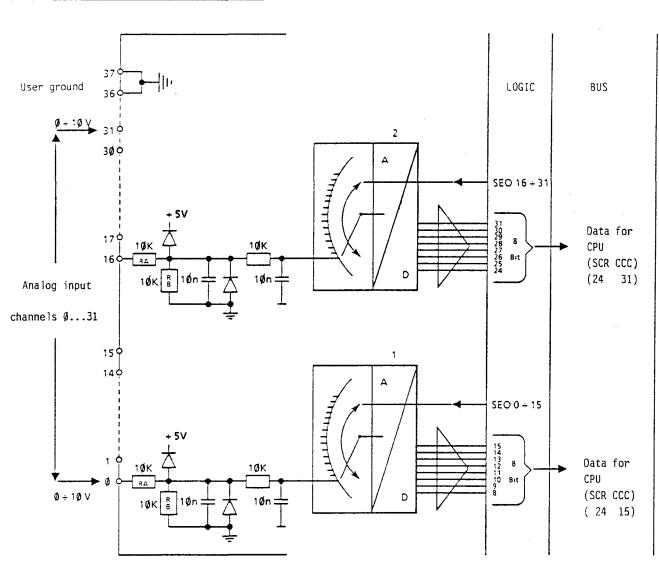
Module addressing

Basic address = \emptyset

Setting of the basic address on the DIL-switch:



Block circuit diagram PCA2.W2..



The block circuit diagram is applicable to type PCA2.W25 with 32 input channels, \emptyset ...1 \emptyset V. For type PCA2.W2 \emptyset with 16 input channels, E16...E31 and the A/D-converter 2 are not provided.

The following changes must be made for the input ranges \emptyset ...5V or \emptyset ...2 \emptyset mA respectively:

Input range	RA	RB	
• Ø1ØV	1Ø K 1 o/oo	1Ø K 1 0/00	Standard
Ø 5V	1ØК 5%	∞	Special
Ø2ØmA	47 Ω 5%	249Ω 1 0/00 ∫	Special

Special versions available on request.

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Overview of binary value/analog value

Standard	Spec	cial
Ø1ØV	Ø5V	Ø2ØmA
+1ØV	+5V	2ØmA
+5V	+2.5V	1ØmA
ØV	Ø) Ø
	Ø1ØV +1ØV	Ø1ØV +1ØV +5V +5V +5V +2.5V

Software

An analog value is read in according to the following steps:

- select input channel
- read in value and store (8 bits)

The input to be read is selected with the instruction SEO n (n = channel number + basic address) by means of a pulse and an analog/digital conversion is triggered. The converted binary value can then be transferred into a counter or flag field.

Example (for software level 1H)

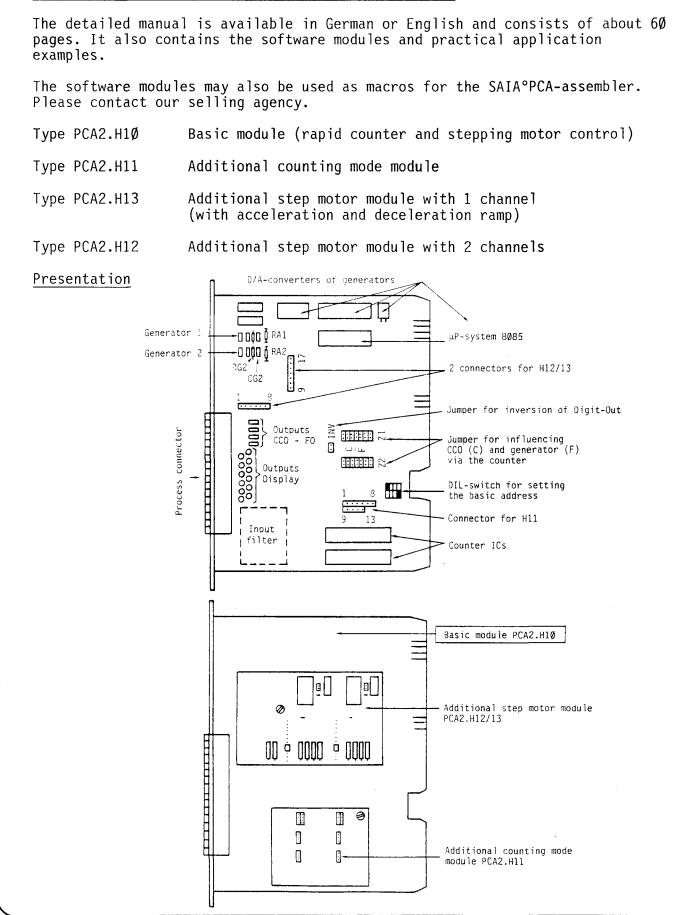
The basic address of the module is \emptyset . The values of the input channels 2 and 18 have to be transferred to the counters C288 or C289 respectively.

	$ \begin{array}{c} \emptyset)\\ 2^{1}\\ 288\\ 15^{1} \end{array} $; Select input channel 2 ; Transfer binary value to C288 ; (the value is in the address field 8 (MSB) to 15 (LSB) 1)
SE0 SCR 24	$ \begin{array}{c} 18 \\ 289 \\ 31 \\ 1 \end{array} $	<pre>Select input channel 18 Transfer binary value to C289 (the value is in the address field 24 (MSB) to 31 (LSB) 1)</pre>

- 1) For a basic address other than \emptyset , the basic address must be added to this operand.
- 2) When using older modules, these program parts should be listed twice for safety reasons.

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B 1.4 Type PCA2.H1.. Counter module for 10...200kHz



B 1.4.1 Type PCA2.H1.. Counter module

Introduction

The registration of signals quickly following one another by means of the standard SAIA°PLC input modules is limited to a frequency of $5\emptyset - 1\emptyset\emptyset$ Hz. On the one hand, this limit is determined by the interference suppression filters of these inputs (typ. 8ms) and on the other hand by the CPU-cycle time in conjunction with the user program. The counter module PCA2.H1.. for processing faster pulse sequences with frequences up to $2\emptyset\emptyset$ kHz is now on offer.

As evident from the following description, the counter module is extremely versatile. Together with two additional modules it allows the following basic functions in two independent systems:

- Rapid counter up to a maximum of 200 kHz (without input filter)

- Incrementing up/decrementing down to the preselected value, 6 digits - Decrementing to zero

- Incrementing/decrementing with recognition of the sense of rotation (decoder)
- Output of programmable frequencies up to 50 kHz
- External display of the counter reading
- Step motor control (clock) with adjustable acceleration and deceleration ramp
- Combination of various functions in the same module

Fields of application:

- Measuring and counting of pulses up to a frequency of 2ØØkHz
 Examples: Pulse generator for velocity, number of revolutions, flow-rate, number of parts, digital measurement of length
- Recognition of the sense of rotation of two-channel incremental shaft encoders

Example: Positioning by means of a DC-motor with a pulse generator flanged to it

- Step motor control Example: Positioning of X-Y-tables, palletizing devices, handling robots

The module PCA2.H1.. has the same dimensions as the I/O-modules. It uses 16 element addresses of the PCA2. The counter module can be operated by means of all CPUs. The module is connected to the process via the $4\emptyset$ -pole plug at the front. The counter module always features two systems which are independent of each other.

The basic module PCA2.H1Ø contains the counter and the generator. An additional counting mode module PCA2.H11 and/or an additional step motor module PCA2.H12/13 can be attached to the basic module.

As is evident from the block circuit diagram which will be shown later, the counter consists in the main of the actual counter, a preselection register and a comparator of counter and register. These 3 circuits are contained in a complex integrated circuit (TC 5070).



Counting and comparing is effected on the counter module itself and not in the user or system programs of the PLC. Moreover, a fast counter output (CCO) is directly influenced by the counter which results in the fast reaction necessary for counting frequencies up to 200kHz. A microprocessor system (8085) assumes the function of administration and coordination between counter module and CPU.

Counter and register are influenced (loaded, cleared) via the user program of the PLC. In addition, various states of counter and register (\emptyset , equal), as well as logic states of elements can be interrogated and influenced via the user program. The respective contents of the counter can be displayed on an external display via the process plug or read into the CPU for processing via the user program.

As mentioned above, the basic module also contains a generator the frequency of which is selected or changed via the user program. The generator can be connected to the counter in order to output a number of pulses predetermined in the register or counter. The generator signal can be registered at the process plug.

On the one hand, the <u>attachable additional counting mode module</u> serves as a phase decoder for decoding the signals of optical angle encoders. Pulses are generated from the dephased signals and the sense of rotation is determined according to which the counter increments or decrements. On the other hand, the pulses of two pulse generators (UP and DOWN) can be processed.

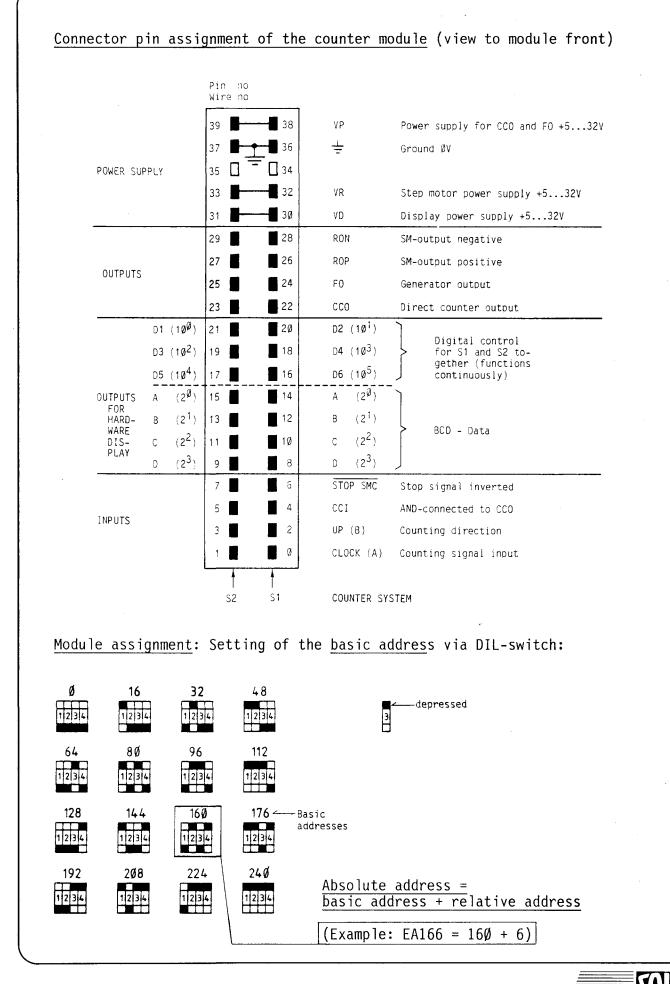
As the name indicates, <u>the step motor module</u> serves to control step motors and due to a high-performance acceleration and deceleration automatics far beyond their start/stop-frequency. The step motor module is connected to the generator of the basic module. The number of steps which the motor has to execute is entered into the counter or the register. The maximum step frequency is supplied to the generator. The start/stop-frequency as well as the ramp slope of acceleration and deceleration is adjusted via a few potentiometers on the step motor module. Now the motor must only be supplied with the start signal and it will execute the steps within an optimal time independent of the PLC system or user program.

The output signal of the step motor module is a one-phase signal. Coding and amplification is effected in the external control electronics of the respective step motor.

It must be mentioned again that the counter module with all its additional modules functions $\underline{a} \ \underline{u} \ \underline{t} \ \underline{o} \ \underline{n} \ \underline{o} \ \underline{m} \ \underline{o} \ \underline{u} \ \underline{s} \ \underline{l} \ \underline{y}$. The user program serves only to supply the module with the information what to do, how and when.

However, it has to be considered that the entire counter module (systems 1 and 2) is to be dealt with only in a single parallel program.

Hardware Block circuit diagram of the counter module PCA2.H1.. STOP SMC ROP Step motor module RON PCA2.H12/13 Generator ZERO F FO F0 EOUAL Register ZERO 000 & REG CCO EQUAL CCI * * * * SAIA°PLC Comparator BUS Counting A (Clock) Counter mode Ζ module B (Up/down) 0 PCA2.H11 DIGIT OUT BCD-OUT 4 ROP = Ramped Output Positive S1/S2 = Entire system RON = Ramped Output Negative F1/F2 = Generator F0 = Frequency Output (generator output) CC0 = Counter Controlled Output REG 1/2 = Register Z1/Z2 = Counter (direct counter output) CCI = Counter Controlled Input (AND-connected to CCO) SMC = Step Motor Control



<u>Counter (Z)</u>	
Number of systems	2 (i.e.: all functions listed in the following are present in double and consequently independent of each other)
Counting frequency	standard: 1ØkHz max.: 2ØØ kHz by adapting or leaving out the input filter
Number of decades	6
Storage of data	registers of the counter module are vola- tile, but data can be saved in non- volatile PLC-registers
Counting direction	forward, backward
Counter = register	selectable via jumper to pos. "C-C=R" (EQUAL) (CCO - counter = register)
Counter = Ø	selectable via jumper to pos. "C-C=Ø" (ZERO) (CCO - counter = Ø)
Direct counter output	1 (CCO = Counter Controlled Output) Switch on via user program Switch off in case of EQUAL or ZERO
Display of the counter contents	via 10 outputs - 4 BCD-out, 6 digit-out (for external power supply) Both systems share the 6 digit-out outputs
Inputs	Clock (A) Up/down (B) H = up; L = down min. 50µs ("H") ARising edges are decisive
	<pre>B CCI (Counter Controlled Input) AND-connected to CCO STOP SMC (for step motor control) all inputs may have a source voltage of 24V, 1ØmA* L = Ø+4V, H = +19+32V* Input delay 5Øμs</pre>
<pre>*) Smoothed DC-voltage</pre>	

Outputs	CCO and FO (Frequency Output) + switching, 532V, 5ØØmA* Load resistor: 524V: min. 48Ω BCD-out and digit-out + switching, 1Ø32V, 1ØØmA* 51ØV, 5ØmA* Load resistor: 1Ø24V: min. 24ØΩ 51ØV: min. 2ØØΩ
Power supply VP	for outputs CCO and FO 532V smoothed (or pulsating for CCO)
Power supply VD	for the outputs of the display 532V smoothed (permissible ripple content depends on the data of the displays in use)
Power supply VR	for step motor control output ROP + switching, 532V, 5ØØmA Load resistor: 524V: min. 48Ω
• •	if output RON is used, the power source is directly connected to the load and VR is not used - switching, 532V, 1ØØmA Load resistor: 524V: min. 24ØΩ
Element addresses used	16 (total for both systems)
Load counter/register	via user program - from elements (I, O, M, H) - from CPU counters (Cn) - from word register (Rn)
Read counter contents	via user program - to elements (I, O, M, H) - to CPU counters (Cn) - to word registers (Rn)

*) Smoothed DC-voltage

SAIA

Standard: fmax = 1ØkHz ±5% Special: by changing the capacitor CG and/or the resistance RG fmax ranges from a few Hz to 5ØkHz Exact adjustment can be achieved by soldering in a balancing resistor RA Symmetric square wave signal

> via the user program fmax can be subdivided into 255 steps (1...255) (8 bits)

via the user program

via the user program or by means of the counter depending on the position of the jumper "F-C=R" (EQUAL) (Frequency-Counter = Register)

```
or
```

"F-C=Ø" (ZERO) (Frequency-Counter = Ø)

via the user program to output FO (Frequency-Output) Pulse length approx. 50µs

Signal

Generator (F)

Frequency

Frequency selection

Start generator

Stop generator

Single pulse



B 1.4.2 Type PCA2.H11 Additional counting mode module

As an additional module it can be attached to the counter card PCA2.H1Ø and secured by means of a screw, after removing the bridging plug from the counter card.

2

Number of channels

Modes - Phase decoder (M1) - UP/DOWN-mode (M2) can be selected by changing the position of a jumper Phase decoder 2 phases to the inputs A and B Mode "x 4" 1 impulse per edge A and B Mode "x 2" 1 impulse per edge of A Mode "x 1" 1 impulse per cycle UP/DOWN-mode signals at A count up signals at B count down signals arriving simultaneously (within one sampling pulse) are suppressed Sampling frequency 2ØØkHz Counting frequency in mode M1 min. 5ØkHz in mode M2 min. 1ØØkHz

<u>B 1.4.3 Type PCA2.H12/H13 Additional step motor module</u>

It can be attached to the counter card PCA2.H10 and secured by means of a screw as an additional module.

Number of channels	1: PCA2.H13 2: PCA2.H12
Parameters adjustable via 5 pote	entiometers (1Ø-turn) each:
P1: max. step frequency	The max. step frequency is supplied by the internal generator (F_{out}) . P1 serves for adjustment of the synchronisation range of the module PLL-circuit of the module oscillator.
P2: Start/stop frequency	adjustable between 50 and 500Hz
P3: Ramp slope	adjustable 1 : 2Ø Basic value can be determined by solder- ing in a capacitor Standard: 1μF> min. slope: 1ØkHz/s
P4: Ramp symmetry	ratio 1 : 5 to 5 : 1
P5: Pulse length	adjustable from 10 \dots 85 μ s for ROP/RON
Module inputs	
Fout	signal from generator
STOP SMC (Step Motor Control)	Reset of SMC-circuit and switch off ROP/RON via process plug
RESET SMC	like STOP SMC, but via the user program
Module outputs	
ROP (Ramped Output Positive)	+ switching pulse output to the process plug 532V (VR) 5ØØmA
RON (Ramped Output Negative)	- switching pulse output to the process plug 532V (VR) 1ØØmA
RAMP READY	can be interrogated in the user program during pulse output> "L"

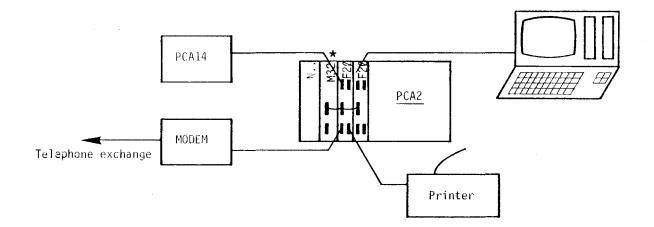


<u>B 1.5 Type PCA2.F2Ø Data line switching module for processor module</u> M22 and M32

<u>Application</u>

The module PCA2.F2Ø allows connecting 4 peripherals which are fitted with a serial interface of the RS 232c-type or a 20mA-current loop.

Via the DATA LINES of the CPU PCA2.M32* data can be exchanged between the SAIA°PLC and these units. Message and control lines allow establishing a connection from or to the respective peripheral unit. Remote transmission via modem is also possible with the data line switching module $F2\emptyset$.



	PCA2.N	PCA2.M32 *	PCA2.F2	PCA2.F2
		$\dot{\mathbf{Q}}$		
		OCPU RUN Oerror	$ \bigcup_{\mathcal{O}} \bigcup_{1}$	$ \begin{bmatrix} 1 \\ 0 \end{bmatrix} $
}		LINES	DATA	DATA LINES
		PGU	$ \bigcup_{2} \bigcup_{3}$	$\begin{bmatrix} 1 \\ 2 \end{bmatrix}$

 *) The data line switching module can be used for the following CPUs: PCA2.M31, M32 and M22. Only M32 will be referred to in the following. For one CPU 1 to 4 F2Ø-modules can be employed, i.e. communication is possible with a maximum of 16 peripherals. 45B

T	· · · · · · ·		
IAC	nnıca		iata
100	mitu	1 0	ιαια

Number of peripheral interfaces

Type of interface

Used addresses

Data transfer

Management of the peripheral interfaces

Number of control and status signals per peripheral interface

Transmission speed

Peripheral connector

Power consumption

Number of modules per rack

4, active or passive

RS 232c or 20mA-current loop, selectable individually

8, the basic address is set with DIL-switches

The data transfer is performed between the CPU PCA2.M32 and the connected peripherals via PCA2.F2Ø

With SEL \emptyset ...3 selection of the peripheral interfaces by means of the user program with the aid of the control and status signals

2 CTS (Clear to Send) RTS (Request to Send)

 $1 \emptyset \emptyset$ baud to max. $96 \emptyset \emptyset$ baud*, defined in the software with the PAS $1 \emptyset \emptyset \text{-in-struction}$

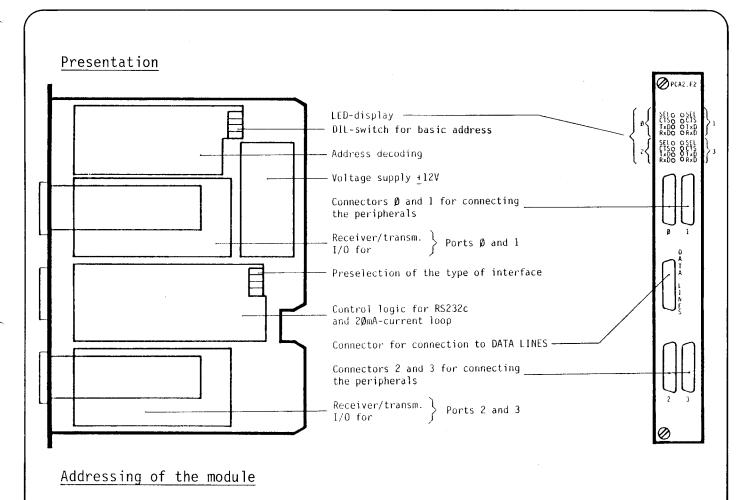
25-pin miniature connector, male (for details refer to "Connector pin assignment")

5V: 480mA (max.) 25V: 45mA + 50mA per active current loop

max. 4 (standard: 1 or 2)

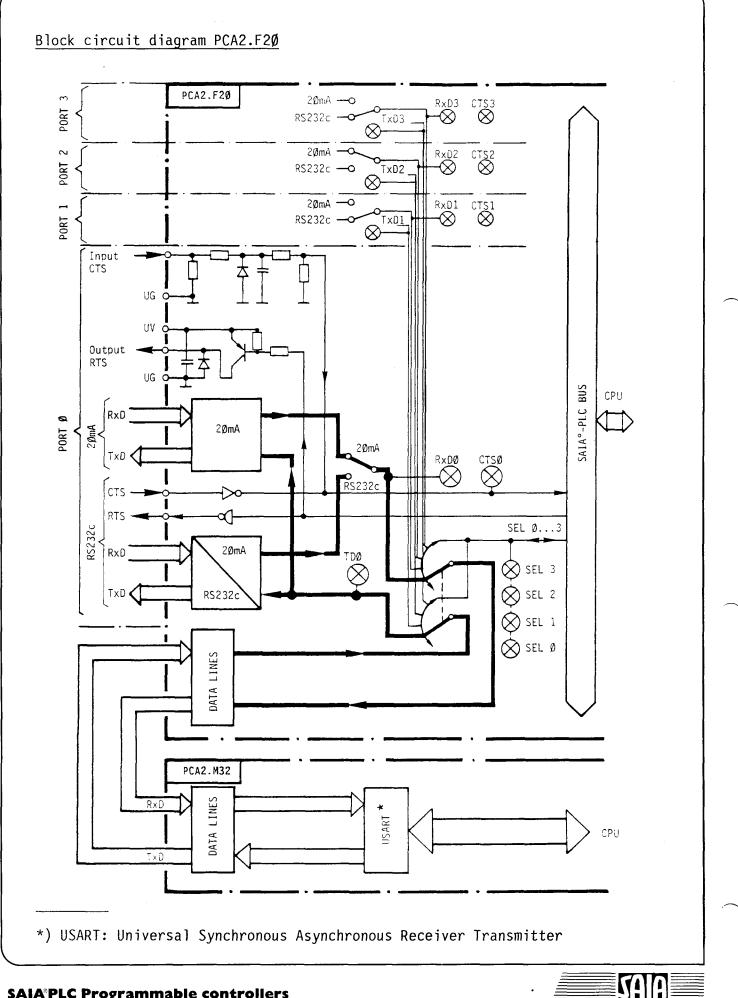
*) In order to obtain high baud rates, the user program must be organised correspondingly (short logic operations).





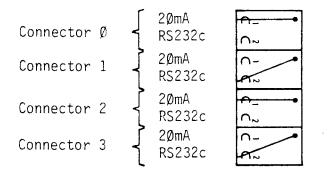
The module uses 8 addresses. As a result, addressing is performed in steps of 8 using 5 DIL-switches.

Ø, 8, 16, 24, 32,, 24Ø, 248 Significance N The basic address (BA) is calculated ----1 as follows: 2 N 4 ω $BA = N \cdot 8; \quad N = \frac{BA}{8}$ OPEN 4 8 J 16 6 The binary value N is set with the 7 not used DIL-switches 1...5. 8 Example for basic address 56 $N = \frac{56}{8} = 7$ Values 1 -N 2 depressed 4 ω Setting of the DIL-switches: 4 8 თ 16 6 N = 1+2+4=7 7 8



Selection of the interfaces 20mA or RS 232c

For each of the 4 peripheral connectors the desired type of interface can be selected. The setting is performed with the fourfold DIP-switch.



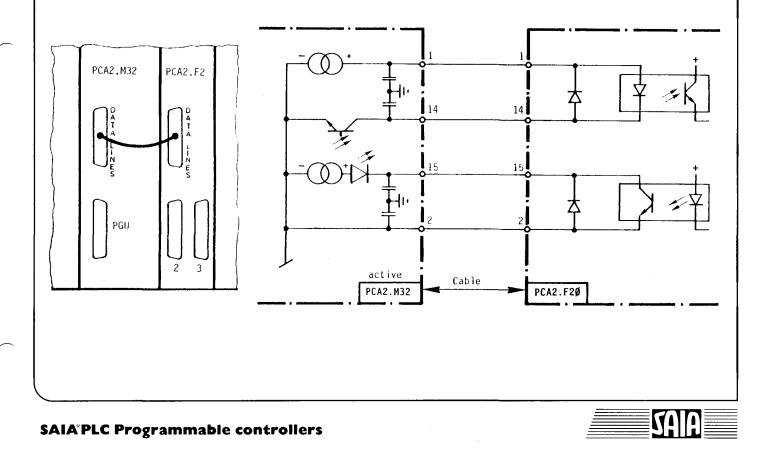
With this setting only the line "Received data" (RxD) is switched. The lines "Transmitted data" (TxD) function simultaneously with both interfaces (see block circuit diagram).

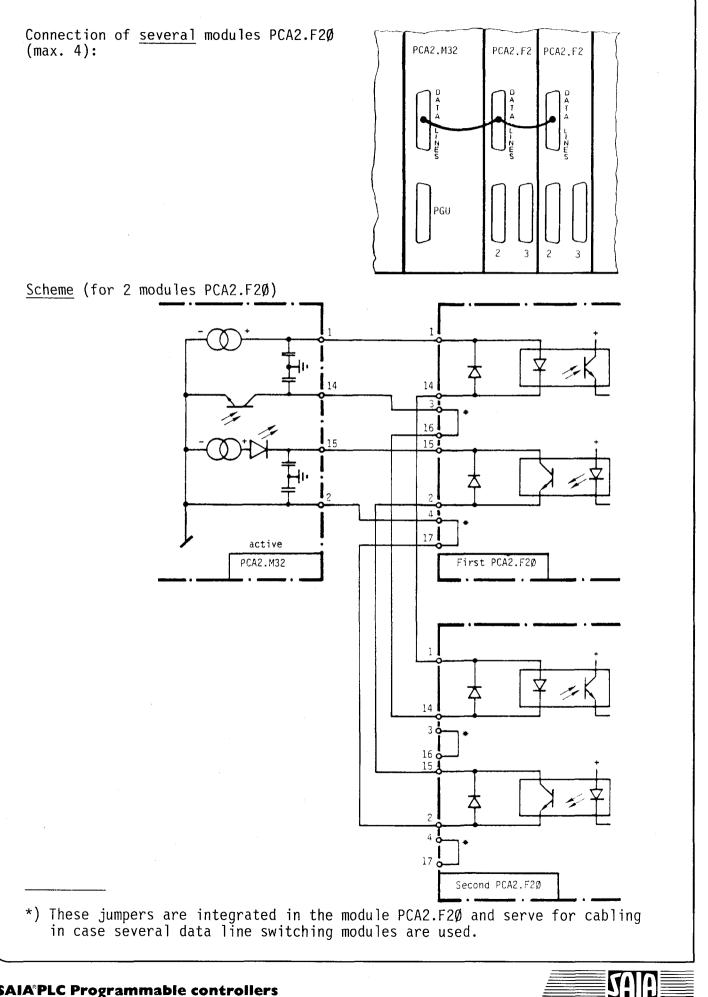
"DATA LINES" connection between PCA2.F2Ø and PCA2.M32

For this connection the interface of the CPU PCA2.M32 <u>must</u> be <u>active</u> (see chapter Hardware M22 and M32).

Connection of one module PCA2.F2Ø:

Scheme





Address assignment and function of the signals

The four peripheral interfaces must be managed via the user program. In order to ensure this, 1 status signal and 1 control signal, which can be set or read in the user program, are available for each connector.

Address assignment

Address	Signal designation	Treatment	
Ø	SEL Ø		
1	SEL 1	<pre>> settable and readable</pre>	
2	SEL 2		
3	SEL 3		
4	RTS Ø CTS Ø	only settable only readable	
5	RTS 1 CTS 1	only settable only readable	
6	RTS 2 CTS 2	only settable only readable	
7	RTS 3 CTS 3	only settable only readable	

Function of the signals

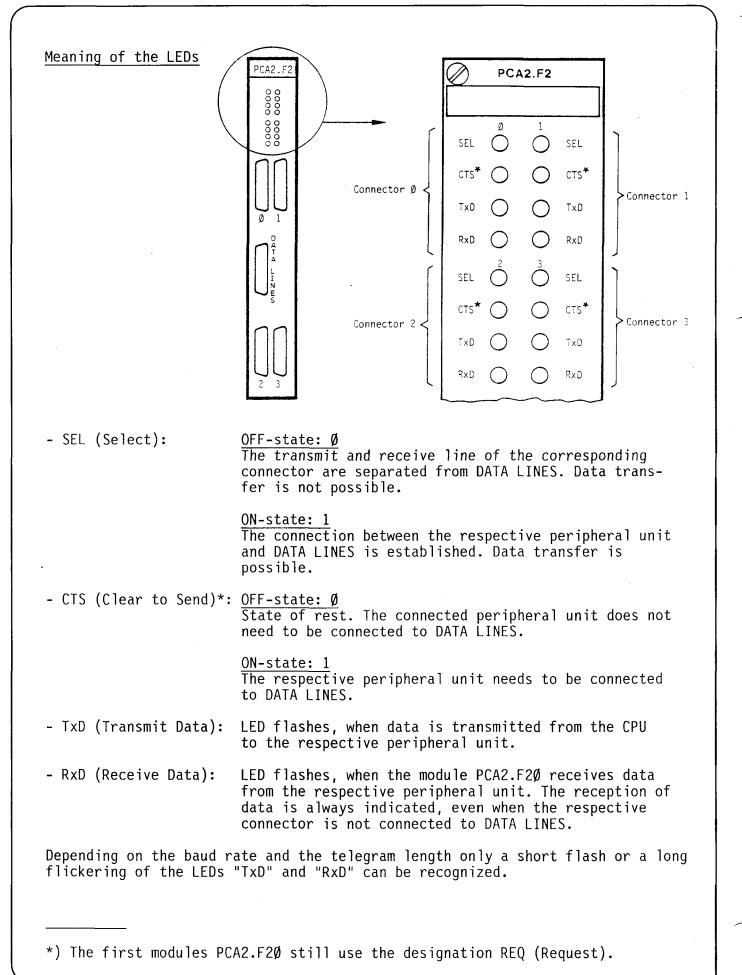
SEL \emptyset ...3 (Select) With the instruction SEO SEL \emptyset ...3 the data lines (TxD, RxD) of the respective peripheral connector \emptyset ...3 are connected to the DATA LINES of the CPU.

With the read commands (e.g. STH SEL \emptyset ...3) it can be determined which peripheral connector was connected to DATA LINES.

RTS \emptyset ...3 With the instruction SEO RTS \emptyset ...3 the respective peri-(Request to Send) With the instruction be informed that the connection to DATA LINES has been established.

CTS \emptyset ...3 With the read commands (e.g. STH CTS \emptyset ...3) it can be determined that a peripheral unit needs to be connected to DATA LINES.

Similar to the input/output module PCA1.B9Ø the control signal RTS and the status signal CTS use the same address. Consequently, one signal can only be set, the other one can only be read (see also "Address assignment").



Interface RS 232c (to peripheral units)

If the interface RS 232c is selected, the data lines as well as the control and message lines of the PCA2.F2Ø correspond to the recommendation RS 232 as regards the function and electric level or they correspond to DIN standard 66Ø2Ø:

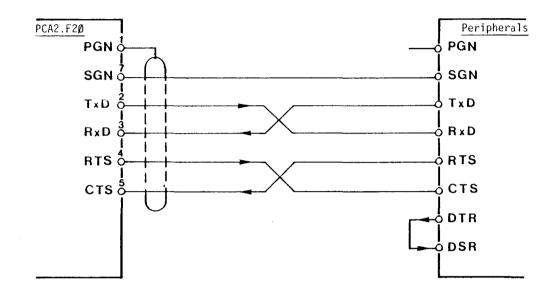
Signal level of the data lines:	"L": +12V "H": -12V
Signal level of the control and message lines:	"L": -12V "H": +12V

Pin assignment according to RS 232c

Pin no.	Abbreviation	Signal name	Direction of the signal
			Periph. PLC
1	PGN	Protective Ground	
2	TxD	Transmitted Data	~
3	RxD	Received Data	
4	RTS	Request to Send	
5	CTS	Clear to Send	
7	SGN	Signal Ground	

Connecting cable for RS 232c-interface (to the peripheral units)

The standardized guidelines hold true for laying the cable, i.e. screened cable with a max. length of 15m (not in the same cable duct as the power cables).



With many peripheral units fitted with RS 232c-interfaces the signals

DTR (Data Terminal Ready)DSR (Data Set Ready)

can be found, too.

In the case of the PCA2.F2 \emptyset they are always assumed to be in the ON-state. For the peripheral unit the connection must be established as evident from the drawing.



20mA-current loop interface (to the peripheral units)

The 2ØmA-interface usually functions without control and message lines. Via the module PCA2.F2Ø, however, up to 4 peripherals are connected to DATA LINES of CPU PCA2.M32. In order to control the data transfer, an output (for RTS) and an input (for CTS) have been provided for each peripheral unit connected.

Signal level of the data lines	"L": 2ØmA "H": ØmA
Signal level of the control lines RTS (output of the type PCA1.B9Ø)	536VDC; I _{max} Ø.5A
Signal level of the message line CTS (input of the type PCA1.B9Ø)	"L": Ø 4VDC "H": 1932VDC

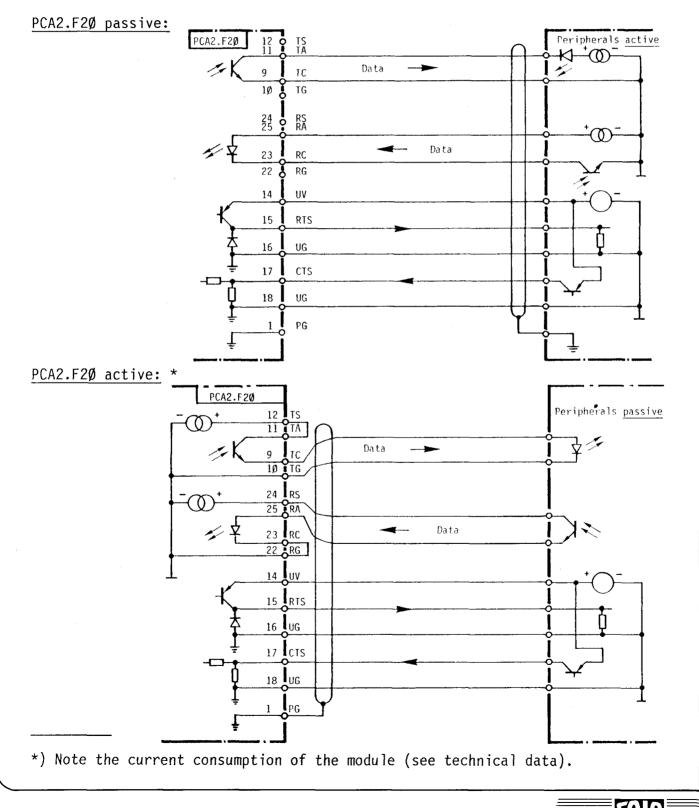
Connector pin assignment for the 20mA-current loop

Pin no.	Abbreviation	Signal name	Direction of the signal Periph. PLC
12	TS	Transmitter Source	}
11	TA	Transmitter Anode	
9	TC	Transmitter Cathode	
1Ø	TG	Transmitter Ground	
24	RS	Receiver Source	
25	RA	Receiver Anode	
23	RC	Receiver Cathode	
22	RG	Receiver Ground	
14	UV	User Voltage	}
15	Output (RTS)	Request to Send	
16	UG	User Ground	
17	Input (CTS)	Clear to Send	}
18	UG	User Ground	

Connecting cable for the 20mA-current loop (to peripheral units)

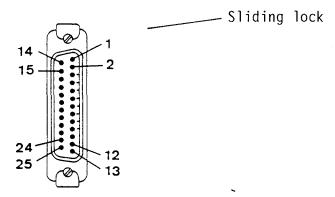
With the $2\emptyset$ mA-current loop good protection against interference for line lengths of up to $1\emptyset\emptyset\emptyset$ m is ensured. In an environment with weak interference fields an unscreened cable can be used.

The connecting cable can be designed in such a way that the peripheral interfaces of the PCA2.F2Ø can be active or passive. In order not to stress the power supply needlessly, we recommend to switch the interface of the peripheral unit to be active (see technical data):



The front connectors of the PCA2.F2Ø

Both the DATA LINES connector and the 4 peripheral connectors are 25-pin miniature connectors, <u>male</u>. They are all fitted with a sliding lock in order to fix the cable connector.



The signal allocation of the connector pins 1...25 for the DATA LINES connector and the peripheral connectors \emptyset ...3 are given in the corresponding chapter.

<u>B 1.6 Selection of power supply modules depending on the power requirement</u> of the PCA2 I/O modules

The power supply modules of the PCA2 meet the internal power requirement of all PCA2-modules at the voltage levels 5V and 25V. When using many modules M32, W1.. and H1Ø, the load limit of the power supply units may be exceeded. In order to avoid this, the nominal load of the power supply modules is compared to the power consumption of the respectively active modules as follows. Note especially the 5V column:

Type	Vin	I for 5	V (A)	I for 25	V (A)
PCA2		max.	average	max.	average
N2Ø	DC	4.Ø	4.Ø	1.Ø	1.Ø
N21	DC	6.Ø	6.Ø	1.Ø	1.Ø
N3Ø	AC	4.Ø	4.Ø	Ø.4	Ø.4
N31	AC	8.Ø	8.Ø	Ø.4	Ø.4

Current load of the PCA2-power supply modules

Power consumption of the PCA2-modules

Type PCA2	I for max.	r 5V (A) average 1)	I for 2 max.	25V (A) average 1)
M32 M21/M22		$\frac{1.14}{\emptyset.62}$	Ø.Ø4 2) Ø.Ø4 2)	Ø.Ø1 Ø.Ø1
R16 R23 (4K) R26/R27/R28/R29	Ø.Ø5	Ø.Ø4 Ø.14 Ø.Ø3		
PØ5/P1Ø		Ø.2Ø		
E1Ø/E11 E2Ø E3Ø E6Ø	Ø.26 Ø.14 Ø.26 Ø.Ø7	Ø.15 Ø.Ø9 Ø.15 Ø.Ø4		
A1Ø A21 A31 A4Ø W1 W2	Ø.34 Ø.16 Ø.21 Ø.34 Ø.85 Ø.Ø8	Ø.29 Ø.Ø9 Ø.15 Ø.29 <u>Ø.67</u> Ø.Ø4	Ø.14 Ø.Ø1 Ø.Ø2 Ø.Ø8 Ø.Ø2	Ø.11 Ø Ø.Ø1 Ø.Ø2 Ø.Ø4 Ø.Ø1
H1Ø H11 H12		Ø.56 Ø.Ø3 Ø.Ø1		Ø.Ø4 Ø.Ø5
F2Ø	Ø.48	Ø.3		Ø.Ø5 ³⁾

1) 50% of all I/O are active

²) With DATA LINES being active

³) Plus 5ØmA per active current loop

SAIA®PLC Programmable controllers

Exampl	е

Туре	I for	5V (A)	I for	25V (A)
PCA2	max.	average	max.	average
M32 2xR26 PØ5 4xE1Ø	1.14 0.10 Ø.2Ø 1.Ø4	1.14 0.06 Ø.2Ø Ø.6Ø	Ø.Ø4	Ø.Ø1
3xA4Ø	1.02	Ø.87	Ø.Ø6	Ø.Ø6
Total	3.50	2.87	Ø.1Ø	Ø.Ø7
Power supply				
N2Ø	4.Ø	4.Ø	1.Ø	1.Ø
N3Ø	4.Ø	4.Ø	Ø.4	Ø.4

It is assumed that never all inputs/outputs are active at the same time. In the above example power supply module PCA2.N20 as well as N30 is sufficient. If the number of I/O-modules is increased at a later stage, however, take care that the power rating reserve is not exceeded.



Chapter B 2

Programming units, additional units and accessories



	ogramming units, additional un	
B 2.1 Add	litional units used for program cumentation)	<u>nming</u> (simulation, starting-up,
uot		
S1Ø Inpu K7Ø Cab P18 Prog PCASS SAIA	l-held programming unit ut simulation unit le gramming unit N°PCA ASSEMBLER DM-copying unit	PCA2.PØ5 PCA2.S1Ø PCA2.K7Ø PCA2.P18 PCASS PCA2.P16
<u>B 2.1.6 N</u>	1emory modules	
	ory module 4K, non-volatile ory module 4K, non-volatile	PCA1.R95 PCA1.R96
<u>B 2.2 Dis</u>	splay modules	
D13 Disp	olay module (remote display) 4 olay interface for D12 olay module (remote display) 2	PCA2.D13
<u>B 2.3 Ext</u>	cernal interface module, type	KOM
KOM 111B	Dual-input interface, 22ØVAC per input	, type D4, output 24VDC/4ØmA
KOM 111B	Dual-input interface, 11ØVAC per input	, type C8, output 24VDC/4ØmA
KOM 121B	Dual-relay output interface,	type M4
	Switching power AC1 : 6A, 25 AC11: 1A, 25	ØVAC (per output) ØVAC (per output)
<u>B 2.4 Dir</u>	mensions of the accessories	
B 2.5/B 2.	6 Dimensions and installation	n of display module PCA2.D12/14

SAIA

B 2.1 Programming units

<u>B 2.1.1</u> Hand-held programming unit PCA2.PØ5

This compact programming unit was developed in particular for the series PCAØ, but it can also be used for the series PCA1 and PCA2.

Programming is performed in the "PROG" - operating mode by means of a 10-part keyboard in simple numerical code. All elements (inputs, outputs, flags, timers, counters) can be quiered or set in the operating mode "MAN".

All timer and counter values can be indicated in the RUN-mode. In the operating mode "STEP" a jump can be effected to any program line (= step address) of the user memory. "BREAK" permits the program processing up to a set breakpoint and continuation in step-by-step operation. For details refer to chapter C "Operating modes".

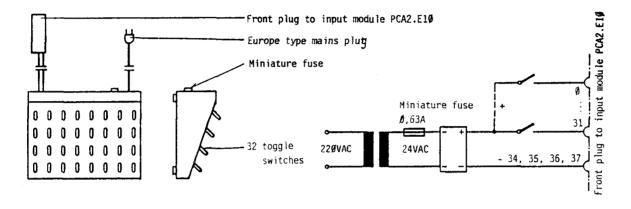
Connecting cable for PGU-connector	
Indication where input is effected	
Display of a program line (7-segment-LED) Display of the accumulator status (ACCU)	STEP CODE OPERAND
Display of the selected operating mode	ORUN ACCU=1 OBREAK OSTEP OTEXT
Keys for the selection of the operating modes	
(inactive on PCA2)	

B 2.1.2 Input simulation unit type PCA2.S1Ø

Its purpose is to simulate input signals via toggle switches so that a program can be tested "at the desk". This considerably facilitates the commissioning of the actual control system.

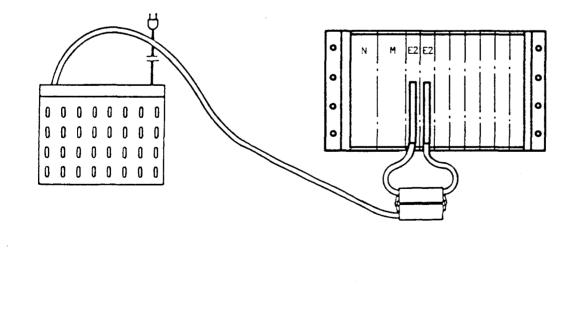
A transformer with rectifier is supplied from a mains cable. From the rectifier is a branch to 32 numbered toggle switches, the signals of which are fed to the PLC inputs via a system cable and plug.

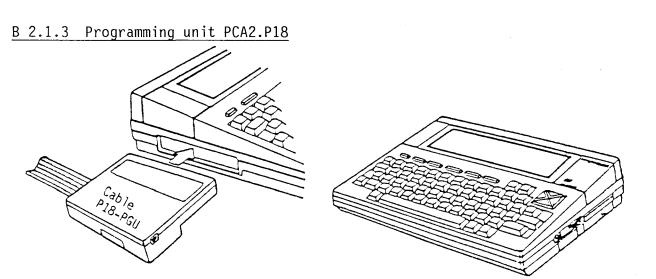
Ordering designation for connection to 220VAC: PCA2.S10 D4



Intermediate cable type PCA2.K7Ø for connection to input module PCA2.E2Ø

As the E2Ø input cards have no joint negative pole and are provided with only 16 inputs, this intermediate cable must be used.





Brief description

The programming unit PCA2.P18 is a compact and versatile means which can be used for programming all SAIA°PLC as well as for servicing.

The P18 uses the commercially available hand-held computer, type NEC 82Ø1A, as hardware. Compactness combined with a high degree of intelligence, an efficient firmware and a variety of peripherals form an ideal portable programming unit, be it on your desk or out in the field.

With the SAIA°PLC connected (via PGU-connector), the P18 makes programming very easy. Moreover, SAIA°PLC texts can be edited or all PLC-registers can be accessed on-line for servicing purposes via the 20mA-data line of the PCA 222 and PCA 232.

In short, the following functions are possible:

- Programming in numerical or mnemonic code
- Display of program sections and texts
- Search functions
- Storage and loading of user programs and texts
- Printing of programs (on an external printer)
- Editing and output of SAIA°PLC texts
- Access to data and registers of SAIA°PLC while user program is running.

Thanks to the permanently stored BASIC-interpreter and the text processing program, the P18 can also be used as a portable personal computer. Numerous additional interfaces and the corresponding software support communication with peripheral units such as printer, modem, tape unit, disk drive unit and bar code reader.

A detailed description is supplied with each unit.

B 2.1.4 SAIA°PCA-ASSEMBLER

The software package SAIA°PCA-ASSEMBLER for comfortable programming, documentation and starting-up

The PCA-ASSEMBLER makes programming of the PCA-family of controllers very easy. The user is efficiently supported in his work by practical menus and the appropriate "HELP" pages which means that he virtually does not require a manual or a knowledge of MS-DOS.

The user program is written in the so-called "Editor" using a conventional text processing program (e.g. Personal Editor or Wordstar). It is possible to use practice-oriented designations for the operands to mark jumps in the form of symbols and labels which are then converted to a PCA-program by the actual "Assembler" and "Linker". Macros with parameters can be implemented for frequently used routines and comments can be used for clearly documenting the new program.

Further possibilities of the new PCA-ASSEMBLER include the modular and global documentation, presentation as flow-charts, an efficient cross-reference list and it is also possible to load the program directly into the RAM-memory of the PCA.

Its advantages become obvious particularly when the controller is started up. In RUN-mode the "Online Debugger" allows the actual states of elements such as inputs, outputs, flags, timers, counters, registers and the date-time to be displayed and also modified. The programs "P1Ø" and "CI" permit direct access to the RAM user memory of all PCAs. By selecting the submenu "Program eproms", tested user programs can be directly loaded into the EPROM programming units PCA2.P16 or ERTEC PGS49.

The software package SAIA°PCA-ASSEMBLER can be run on all IBM-PC/XT/AT or PS/2 or compatible units which fulfil the following conditions:

- 512 KByte main memory

- 2 floppy disk drives of 360K or even better 1 floppy disk drive and a hard disk
- 1 or even better 2 bidirectional, parallel interfaces for controlling a printer and for connection to the PGU-connector of the PCA
- Monochrome or colour VDU (with MCGA, CGA, EGA, VGA or Hercules cards)
- Keyboard as desired
- Operating system MS-DOS 3.0 or a higher version
- Cable PCA2.K43 for connection to the PGU-connector of the PCA
- Text processing program as desired (Personal Editor and Wordstar are recommended)

A detailed description is available for every software package.

The SAIA°PCA-ASSEMBLER software package is available in three complementary packages:

- PCASS1 ONLINE The basic package mainly contains the tools needed for commissioning as well as for writing or modifying program directly in the PCA.

- PCASS2 PROGRAMMING The main package includes the entire PCASS1 package as well as the tools "Assembler", "Linker", "Disassembler", "Textassembler", etc. They allow preparing and documenting extensive programs in various ways by using symbols, labels and macros.

- PCASS3 TRANSFER It includes aids for optimizing communications programs and loading EPROMs.

All software packages are available in German, French or English and, if desired, on a $5 \ 1/4$ " or $3 \ 1/2$ " disk.



Screen

Main menu of PCA-ASSEMBLER

KKKKK S	AIA AG	Marktbereich CH 3	280 Murten жжжжж
Directory: C:\PCASS	· · · · · · · · · · · · · · · · · · ·		16.12.88 13.30
Edit		Text assembler	Compare programs
Assemble		Disassembler	Xref listing
Link		floW chart	File handling
Up⁄download		Runtime analysis	Ms-dos command
Online debug		Hex converter	Setup
comms Interface		Program eproms	Quit

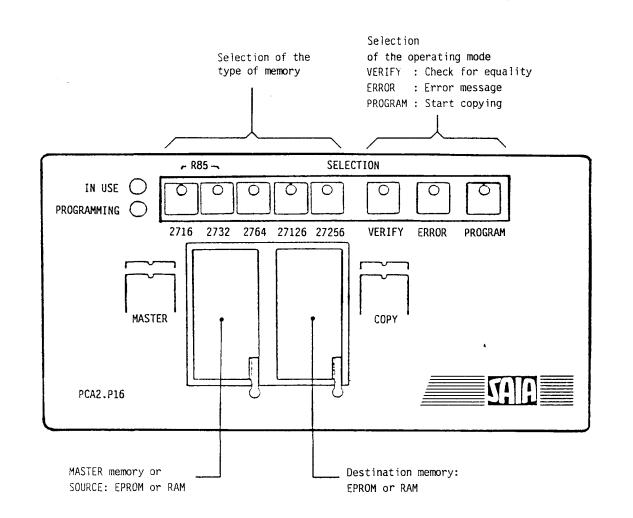
ONLINE DEBUG menu of PCA-ASSEMBLER

C260 2090 e12 3011 0010 B200 EE EF FF 38 67	uy du yy mo dm hh mm ss 48 03 88 12 15 17 05 58
	-Program
23 1101 0000 0100 0011	A 1 03 2
T256 Z16 3	A Z 83 7
	A 3 10 12
	A 4 10 21
	A 5 10 13 A 6 10 24
	A 6 10 24 A 7 14 256
	A 8 00 500
	A 9 01 256
	A 10 10 25
	A 11 ZØ Ø
	L_,
rite	
lay Write Program clock Save	Load comms-Interface Reset

SAIA

B 2.1.5 Type PCA2.P16 EPROM-copying unit

Owing to two high-quality sockets (Textool) the unit can be used for copying and comparing EPROMs and buffered RAMs independently of other units. The serial interface RS 232c permits connection of any commercial personal computer. A program supporting operation of the P16 from the IBM-PC is part of the PCAassembler (package no. 3).



The P16 meets especially the requirements of the SAIA°PLC. In addition to the usual EPROM types 2716 to 27256, the buffered RAMs PCA1.R95 and PCA1.R96 can be written to and read.

A detailed manual is delivered with each unit.

Technical data

Supply voltage Power requirement

Microprocessor

Dimensions

Weight

Serial interface

22Ø VAC 5Ø Hz ± 1Ø% 2Ø VA MC 68Ø9 RS 232c (96ØØ, 24ØØ, 12ØØ and 3ØØ bauds) 222 x 47 x 172 mm (W x H x D) 1.7 kg

The following memory modules can be programmed with the P16:

Туре	Progr	amming	voltage
2716 2732 2732A 2764 27128 27256	25V 25V 21V 21V 21V 21V	1) 3) 1) 2)	
2816		3)	
PCA1.R95 (buffered RAM)			
PCA1.R96 (buffered RAM)			

- ¹) For the type 2732A the P16 has been set to a programming voltage of 21V (factory setting). For the type 2732 which has a programming voltage of 25V, a jumper needs to be re-soldered on the pc-board EP 8Ø Ø67.
- ²) For the type 27256, which has a programming voltage of 12.5V, the resistor R3 (3k6) needs to be changed to 2k on the pc-board EP 8Ø Ø66.
- 3) Do not use with SAIA°PLC.

Copying

During copying, data is read from a master-IC and written to a copying-IC. When working without the Personal Computer, i.e. without using the serial interface, copying can usually be performed only using the same types of EPROM. However, mixed operation is possible using the EPROM 2764 and buffered RAMs PCA2.R95 or PCA2.R96. Only the <u>entire memory contents</u> can be copied from the MASTER socket to the COPY socket.

- 1. Select the copying EPROM with the appropriate key. The corresponding LED lights up. For the EPROM-emulators R95 and R96 the keys 2716 and 2732 must be pressed simultaneously.
- 2. Insert the master-IC and the copy-IC in the frames. Take care that the notch or pin 1 respectively is at the top on the left. The ICs are retained in the frames by pressing down the levers. In the case of the 24-pole ICs it must be noted that the <u>upper</u> contact openings must not be covered.



3. Press key 'PROGRAM'. The LED 'IN USE' lights up for a short time. During this time a check is performed to determine whether the memory module to be programmed has been erased. Afterwards the LED 'PROGRAMMING' also lights up until programming is finished. Any errors which occur during programming, are displayed by the flashing LED 'ERROR'. Moreover, an LED lights up in the keys indicating the type of error.

Error messages

Key 2716 : EPROM cannot be programmed Key 2732 : EPROM has not been erased Key 2764 : EPROMs are different Key 27128: EPROMs are different and copy-IC empty Key 27256: 2816 cannot be erased

The error display is cleared with the key 'ERROR'.

Comparing

The procedure is similar to copying. However, the LED 'PROGAMMING' does not light up. Proceed as follows:

1. Select copying-EPROM with the appropriate key.

2. Press key 'VERIFY'.

If no error message appears, the contents of the two memory modules are the same. The flashing LED 'ERROR' indicates an error (see list of errors).

Erasing the 2816 (EPROM)

In order to erase the 2816, press the key 'ERROR' and '2716' simultaneously.

Important: The memory module 2816 cannot be used together with SAIA°PLC.

When the PCA2.K46 cable is used, the transfer of data is supported under menuguidance by the SAIA°PCA-ASSEMBLER with the "Program eproms" program (in package no. 3).

B 2.1.6 Type PCA1.R95/R96 Buffered RAM chip

RAM-memories are read-/write-memories, which means that the information can be modified at any time with the aid of a programming unit (as data memory in the PCA2 also via the user program).

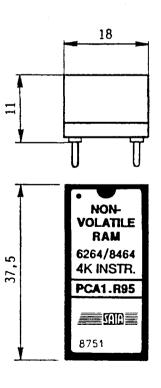
The buffered RAM chip is the ideal memory chip serving as a program and text memory from the programming stage to the start-up. Owing to the incorporated buffer battery and the protective electronic system, this memory chip can be detached from the PLC and transported without modifying its contents.

The slightly conductive plastic socket protects the pins against static charges, thus avoiding memory content changes. The internal battery is thereby not discharged.

Memory type	PCA1.R95	PCA1.R96
Storage capacity		
- Program lines - Texts, data	4К 8К	4К 8К
Number of pins	28	28
Buffer battery life	approx. 8 years	approx. 6 years

Application in PCA14/15, PCAØ and PCA2.

Presentation



SAIA®PLC Programmable controllers

B 2.2 Display modules

B 2.2.1 Type PCA2.D12 Display module

<u>General</u>

The PCA2.D12 module is a remote display which can be controlled via SAIA°PLC outputs. It has a 4-digit display and is able to indicate a decimal point. The display can be built in anywhere at a greater distance to the PLC e.g. in the door of a control cabinet or an operating panel. Due to data transmission being effected via outputs, several displays can be controlled by one PLC. In conjunction with the display interface PCA1/2.D13 the D12 can be connected even at a greater distance to the PGU-connector where the comfortable instructions DTC and DOP are available.

Structure, function

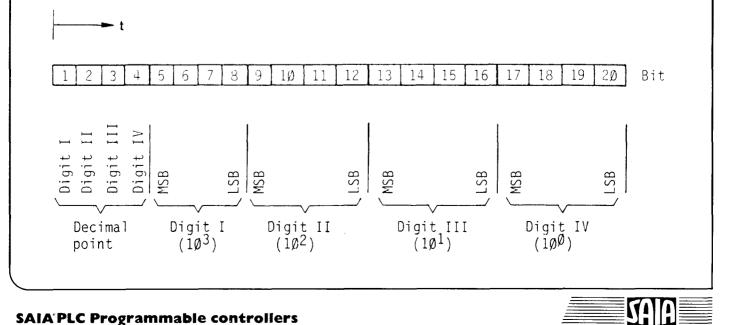
The module is in the same housing as the electronic totalizing counter of the CKG type. It consists of the following main components:

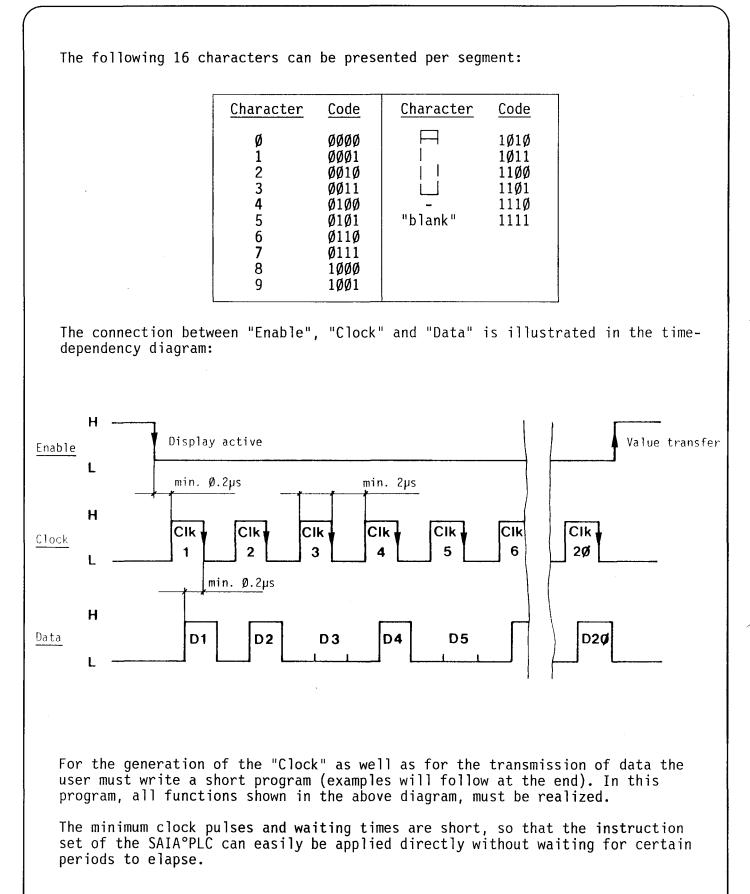
- power supply 24VDC
- 3 inputs for 24VDC
- decoder/driver
- 4-digit, 7-segment display with decimal point

The 3 outputs of the PLC resp. the 3 inputs of the display are designated "Enable", "Data" and "Clock". The <u>Enable signal</u> activates the display, i.e. Enable = "L" --> display is able to receive data, Enable = "H" --> display is inactive (it is not able to receive new data). Via the <u>"DATA"</u> line data in BCD-format is transmitted sequentially, i.e. bit by bit from the SAIA°PLC to the display. The display accepts each bit with the falling edge of the <u>"Clock"</u> signal.

For a complete indication (4 digits with or without decimal point) always $2\emptyset$ clock signals must be generated and $2\emptyset$ data bits must be transmitted (4 BCD-values + 4 bits for the decimal point).

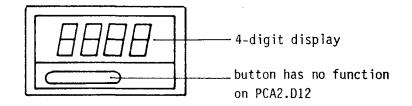
The following sequences of the 2Ø data bits must be adhered to:

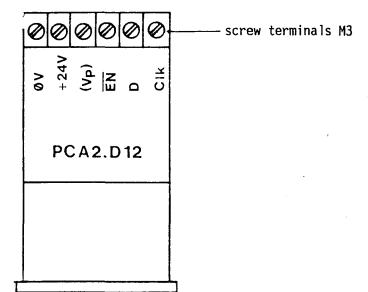




SAIA[®]PLC Programmable controllers

Presentation and terminal arrangement





Technical data:

- Supply voltage
- Input voltage for EN, D, CLK
- Input current for 24VDC
 Definition of the input voltages
- Input delay
 Usable SAIA°PLC output modules
- Control
- Connection V_P
 Dimension drawing see chapter B2.5

24VDC \pm 20%, two-way rectification is sufficient

24VDC, smoothed

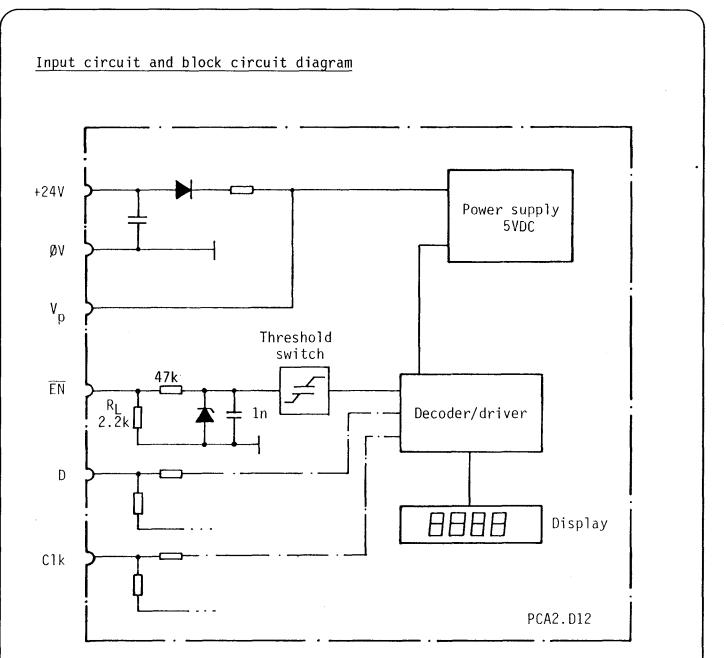
1ØmA

"H": 19V...32V "L": ØV... 4V

< 1ms PCA1.A1Ø, B1Ø, B8Ø, B9Ø PCA2.A4Ø

serially via 3 PLC-outputs or via interface D13

Output, used to supply D13 with voltage

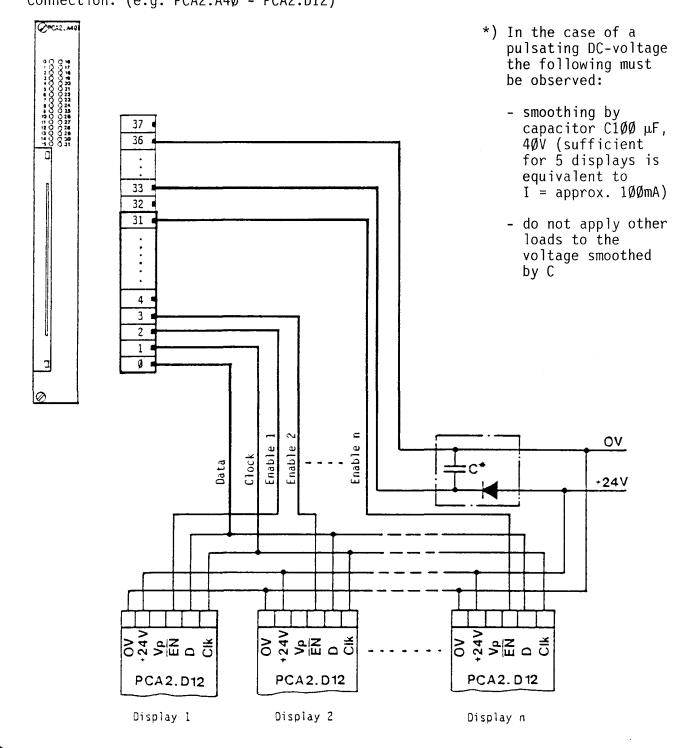


Note:

 $V_{\rm p}$ supplies display interface D13.

Connection of several displays to a PLC

Since the PCA2.D12 module is able to transmit an "Enable" signal, i.e. it can be switched to be active or inactive, <u>the same "Clock" and "Data" signals can</u> <u>be used for several displays</u>. These are transmitted to each display simultaneously. The "Enable" signal decides which display is controlled. This means that for <u>each display one</u> "Enable" signal is necessary (1 output per display). This also means, however, that for as <u>many displays as desired</u> only <u>one data</u> and one clock output must be provided.



Connection: (e.g. PCA2.A4Ø - PCA2.D12)

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Examples

Example 1

<u>Six PCA2.D12 displays</u> are to be connected to one SAIA°PLC. How many outputs are required?

Solution 1

Per display module one "Enable" signal6 outputs1 "Data" signal (simultaneously to all display modules)1 output1 "Clock" signal (simultaneously to all display modules)1 output

<u>Total</u>

8 outputs

Example 2

Every half second a counter is to be incremented up to the value 9999 and then reset to zero. Its content is to be indicated on the PCA2.D12 display module with a decimal point in the 2nd place.

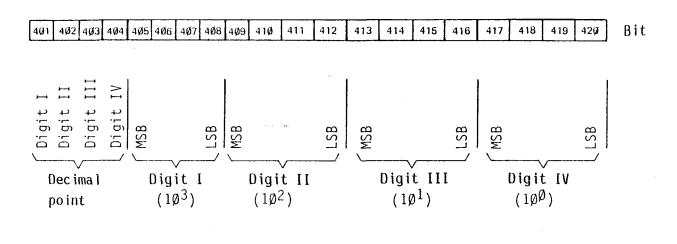
The following outputs must be assigned for "Enable", "Data" and "Clock":

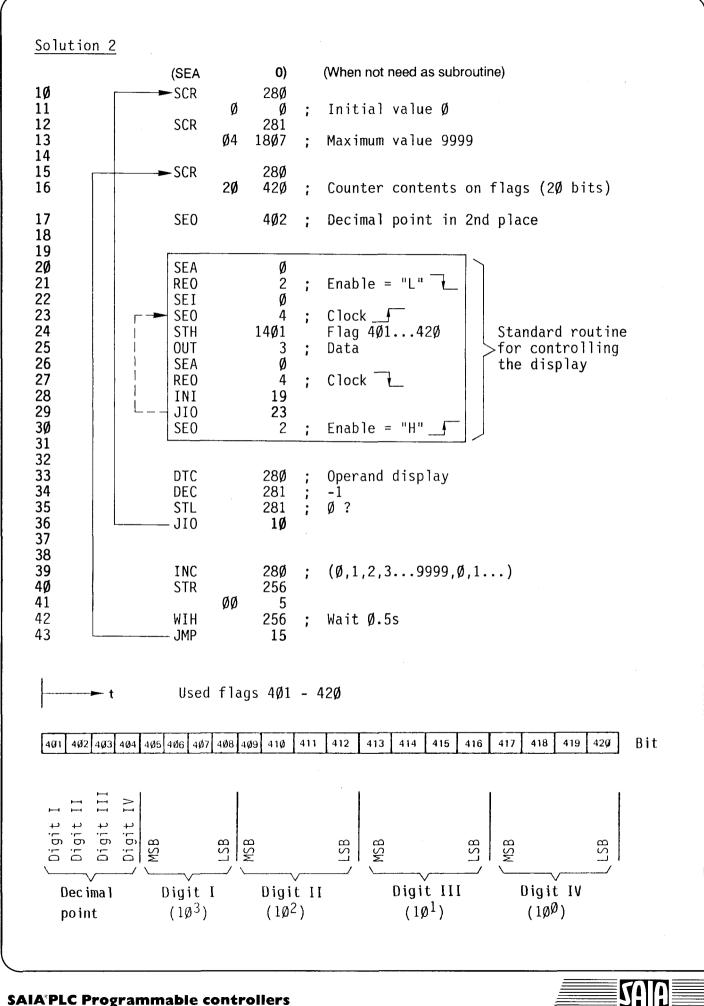
EN : 02 D : 03 CLK: 04

Used counters: C28Ø C281

► t

Used flags 401 - 420





SAIA[®]PLC Programmable controllers

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B 2.2.2 Type PCA2.D13 Display interface

Description

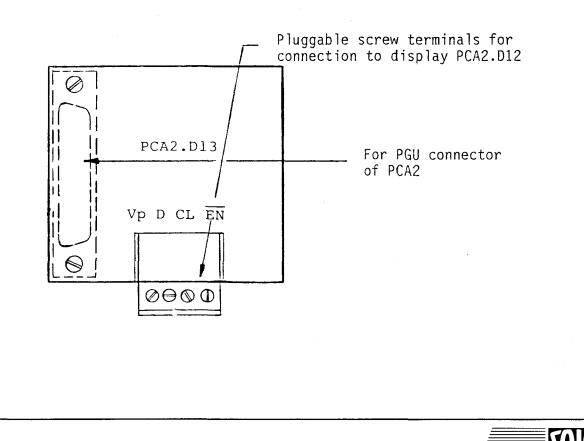
The display interface D13 combines the advantages of the display module PCA1.D11 for PCA1 (simple software handling via the instruction DTC and DOP for 4-digit decimal displays) and those of the display PCA2.D12, which need not be located anywhere near the SAIA°PLC.

The D13 is inserted in the PGU-connector of the SAIA°PLC and connected to the display PCA2.D12 by means of pluggable screw terminals.

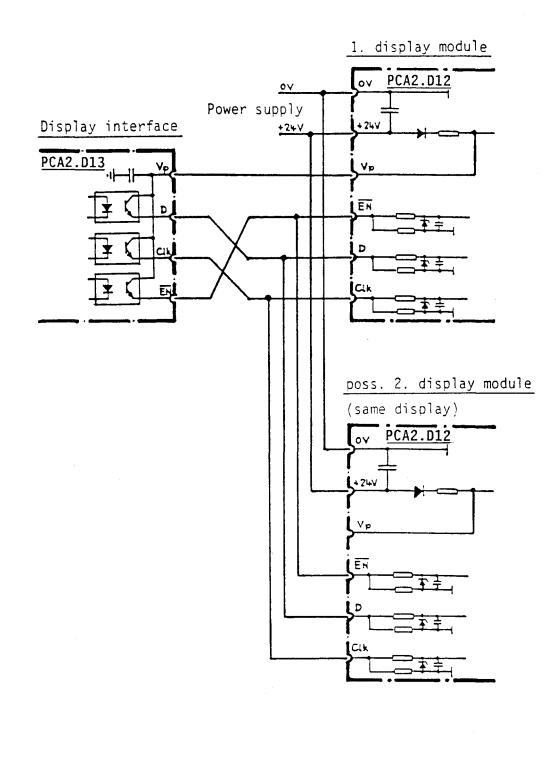
Technical data

- Supply voltage Vp: 24VDC, ±20%, full-wave rectified is sufficient (supplied by the display module PCA2.D12)
- 3 opto-isolated outputs for EN, D, CLK
- Connection of 2 displays PCA2.D12 is possible (same display)
- Control by means of the instructions DOP and DTC (see manual Software 1H)
- Concerning the cable layout and type of cable between D12 and D13 no special measures are required. The same general criteria as for the cabling of input and output modules apply (see chapter A 8).

Presentation

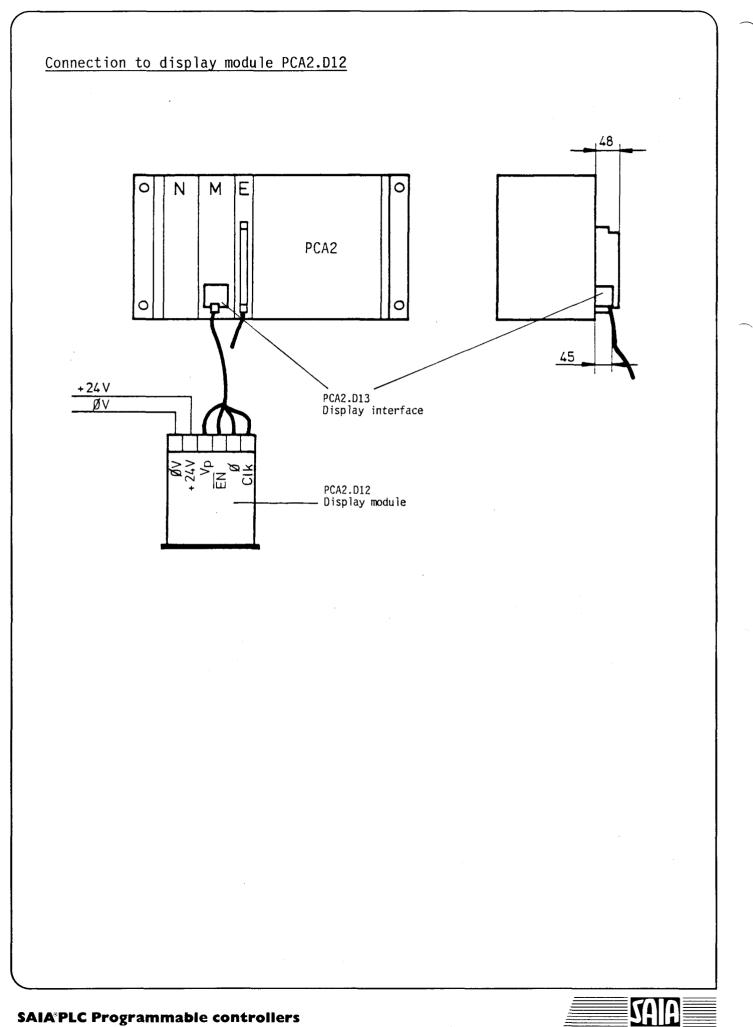


Connection diagram

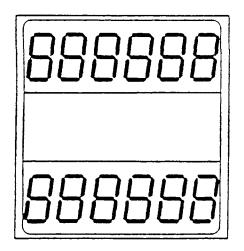


Note:

- Both displays indicate the same data.
- Module D13 is supplied by module D12 backwards via the terminals Vp. This and the use of optocouplers ensure maximum interference protection of the PCA2.



<u>B 2.2.3 Type PCA2.D14 Display module</u>



General

The PCA2.D14 module is a remote display module which is controlled via 3 outputs of the SAIA°PLC. The module has two 6-digit displays. Several PCA2.D14 can be connected in series in case of more than two displays.

Application, control

The module was developed in connection with the fast counter module PCA1.H1Ø. In this application controlling is performed by the counter module alone. The user must only program the appropriate mode in the user program.

When the PCA2.D14 is used without the H1Ø module, the information to be displayed is most easily transmitted serially with a standard program routine from a flag field via 3 SAIA°PLC outputs.

Technical data

Display Digit height Supply voltage

Input voltage for EN, D, CLK Input current at 24VDC Definition of the input level

Input delay Usable SAIA°PLC output modules

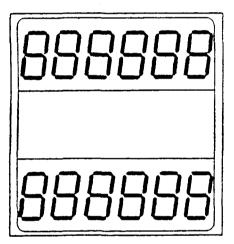
Control

2 times 6 digits, 7-segment LED 10mm 24VDC ± 20%, full-wave rectified is sufficient 24VDC smoothed 10mA "H" = +19...+32V "L" = 0...+4V < 1ms PCA1.A10, B10, B80, B90 PCA2.A40 serially via 3 SAIA°PLC-outputs irrespective of the number of D14 Structure, function

The module is located in the same housing as the electronic totalizing counter CKG/AC.

Terminals: Screw terminals combined with connection strips (2.8 x \emptyset .8 mm) for flat pluggable bushes or soldering.

PLC-output	Clock	>	Clk	
PLC-output	Data-In	>	D-IN	
PLC-output	Enable	>	EN	
Carry	Data-Out	>	D-OUT	PCA2.D14
Voltage supply	+24V	>	+24V	
Voltage supply	ØV	>	ØV	



Upper display

Lower display

The data for a display of 2 x 6 digits are most easily presented in a complete flag field, e.g. M500...547 in BCD-notation. If these values are kept in counters, they must be transferred to the flag fields first.

500 M o o o o MSB LSB 100'000	0000 1Ø'ØØØ	0000 1'ØØØ	0000 1ØØ	0000 1Ø	523 0000 MSB LSB 1	upper display
524 M o o o o MSB LSB 1ØØ'ØØØ	0000 1Ø'ØØØ	0000 1'ØØØ	0000 1ØØ	0000 1Ø	547 0000 MSB LSB 1	lower display

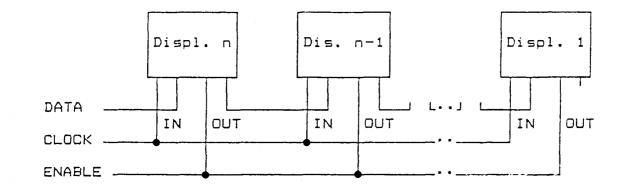
Software routine

Every time the following routine has been executed the current information in the flag field is indicated on the display until the display is updated by a new piece of information after a further run.

Softlevel 1 *

(6Ø 61 62 63 64	SEA REO SEI SEO SCR ØØ	Ø) 2 Ø 3 28Ø 4	ENAB DATA AUX.				(When <u>not</u> u	used as subrou resses	tine)	
66 67 68 69 7Ø 71	SEO REO DEC STH JIO SCR	4 28Ø 28Ø 66 28Ø	AUX.				Enable Data Clock Flag Aux. cour	O2 O3 O4 M5001	М547	
73 74 75 76 77 78 79 8Ø 81 82 83	OUT SEA SEO REO JIZ DEC STH JIO JMP	16 15ØØ 3 Ø 4 4 4 4 7 84 28Ø 28Ø 73 63	AUX.	K K COUNTER COUNTER				(upper and	index regis l lower splay) **	ter
84 (85	SEO RET	2 Ø)	ENAB	LE			(When use subroutin			
500 M o o MSB 100	oo LSB VØØØ	оос 1Ø'(0000 1'ØØØ	0000 1ØØ	0	0000 1Ø	523 0000 MSB LSB 1	upper display	·
524 M o o MSB 1ØØ	LSB	000 1Ø'\$		0000 1'ØØØ	0000 1ØØ	0	0000 1Ø	547 0000 MSB LSB 1		
*) The display module D14 can thus be controlled from any SAIA°PLC (including PCA13 and PCA21)										
**) For connecting several D14 in series see following page.										

The following diagram shows several PCA2.D14 connected in series: Each D14 displays its own data.



The flag field containing the information to be displayed must be expanded correspondingly:

for 1 PCA2.D14 = 1 x 48 flags for 2 PCA2.D14 = 2 x 48 flags for 3 PCA2.D14 = 3 x 48 flags etc.

The routine in the user program remains the same, only the instruction "INI" must be changed accordingly:

for 1 PCA2.D14 = INI 47 for 2 PCA2.D14 = INI 95 for 3 PCA2.D14 = INI 143 etc.

In other words, INI $(n \times 48) - 1$ with n = number of PCA2.D14.

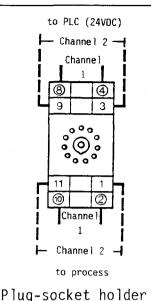
The following 16 characters per segment can be presented:

 Character	Code	<u>Character</u>	Code
Ø 1 2 3 4 5 6 7 8 9	ØØØØ ØØ10 ØØ11 Ø100 Ø101 Ø110 Ø111 1ØØØ 1ØØ1	H I I - "blank"	1Ø1Ø 1Ø11 11ØØ 11Ø1 111Ø 1111
 · · · · · · · · · · · · · · · · · · ·			



B 2.3 KOM series external interface module

The purpose of the external interfaces is for adapting the I/O levels of the PLC from 24VDC to the process requirements. They are constructed in two-channel form and mounted in plug-in housings for an 11-way round socket. LEDs indicate the logic status ("H" = ON), facilitating the rapid checking of the signal lines as far as the terminals of the process. To render the wiring easy to view, the cables from the process or to the PLC are arranged on the opposite side of the plug holder.



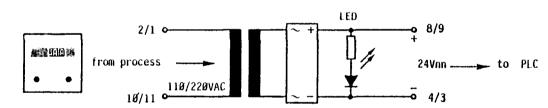
Order no. 4'408'4817'0

B 2.3.1 Type KOM 111B Dual input interface

The purpose of this input interface is for the isolation of the mains control lines from the 24V signal level of the PLC. The isolation is accomplished by means of inductive transmitters; this has the advantage of providing a safeguard against surge voltages.

Front

Switching scheme (per channel)



Technical data

Input voltage

Input current

Output voltage

Output current

Reaction time

Surge voltage on process side

Connection

Order specification

22ØV, 5Ø...6Ø Hz ± 2Ø% type KOM 111B D4 11ØV, 5Ø...6Ø Hz ± 2Ø% type KOM 111B C8 in each case Ø.5A 24VDC pulsating in each case max. 4ØmA max. 1Øms (acc. to phase length)

5kV, 1/5Ø μs

11-way round socket

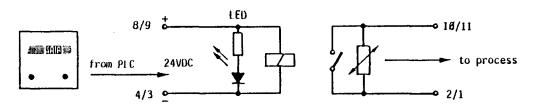
KOM 111B D4 or C8 (see input voltage)

B 2.3.2 Type KOM 121B Dual-relay-output interface

Electric isolation in this interface is achieved by relays, the contacts of which are able to directly switch mains voltages. The normally-open contact to the relay is used corresponding to the PLC output.

Front

Switching scheme (per channel)



Technical data

Input voltage

Input current

Relay contact

Switching power

Contact life (AC1)

Order specification

24VDC \pm 20%, smoothed or pulsating

20mA respectively

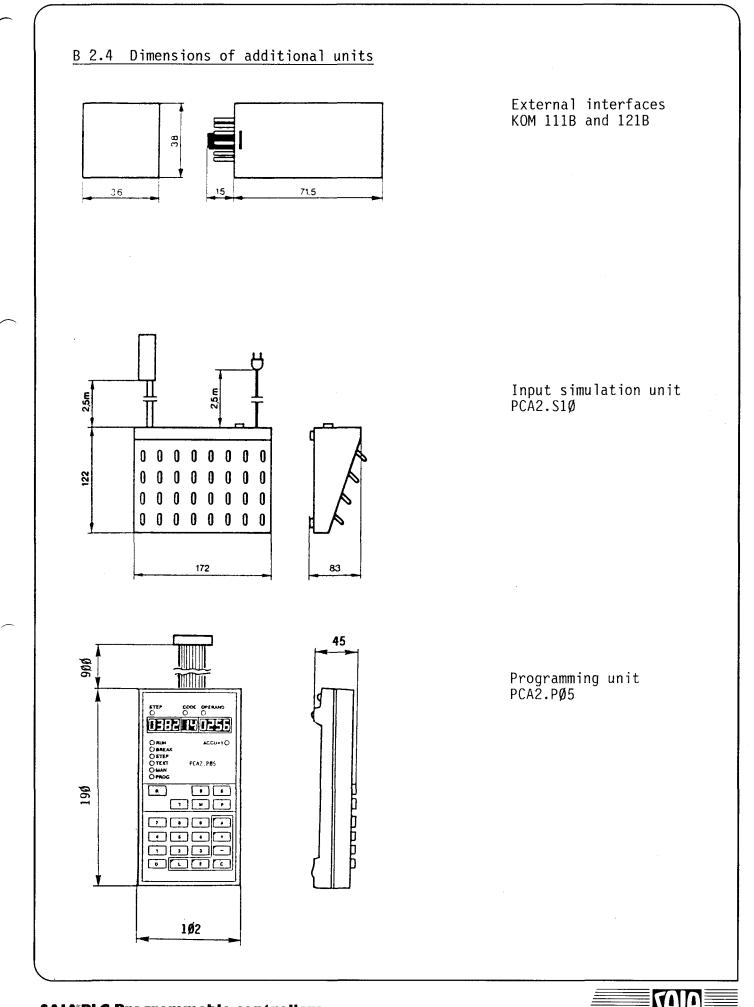
1 normally-open contact with hard silver contacts respectively

6A, 25ØVAC AC1 1A, 25ØVAC AC11 respectively

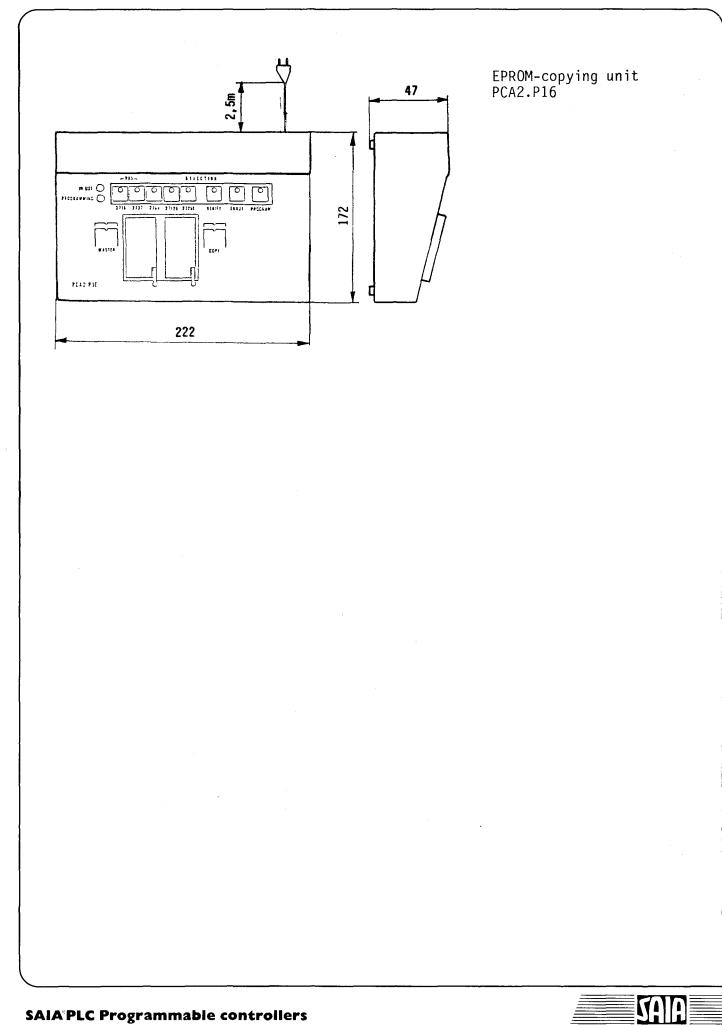
3A, 22	2ØVAC	Ø.1	mio.	switching	cycles
1.5A,	22ØVAC	Ø.5	mio.	switching	cycles
Ø.3A,	22ØVAC	5	mio.	switching	cycles

KOM 121B M4

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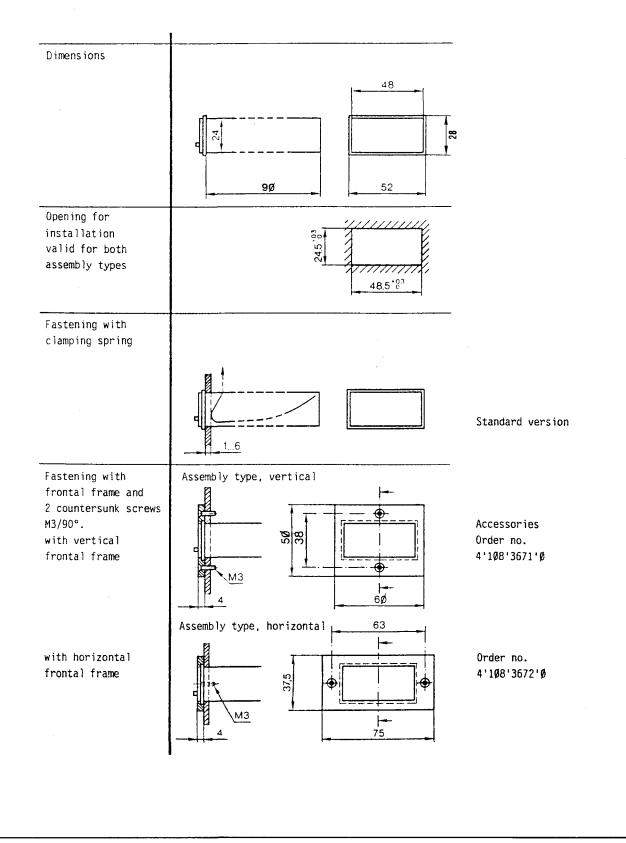


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B 2.5 Dimensions and installation of PCA2.D12

The display module can be installed in any position desired anywhere in a control cabinet door or an operating panel.

The display can be fastened in three ways:



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B 2.6 Dimensions and installation of PCA2.D14

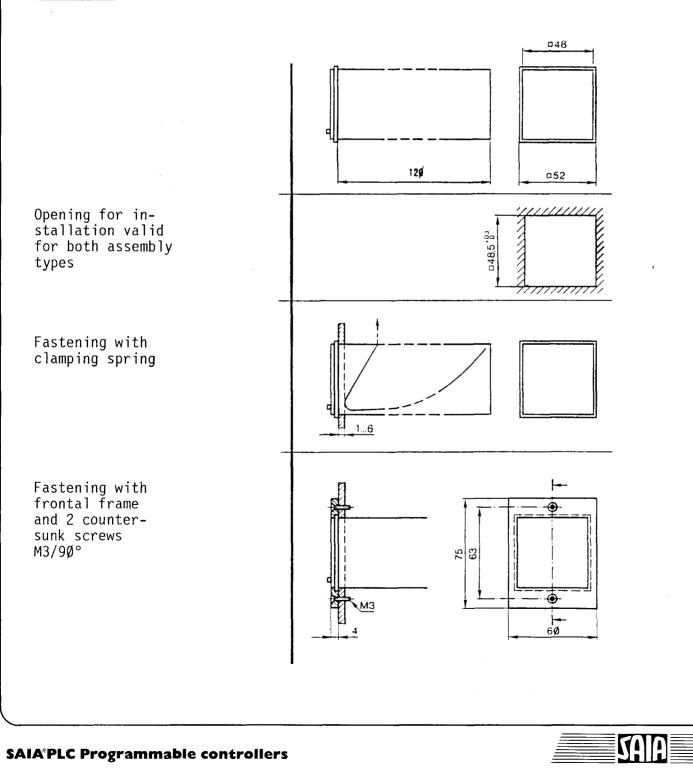
The display module can be installed in any location desired.

It can be fastened in two ways:

with a clamping spring
with a frontal frame and screws

(The clamping spring and the frontal frame are supplied with every PCA2.D14).

Dimensions

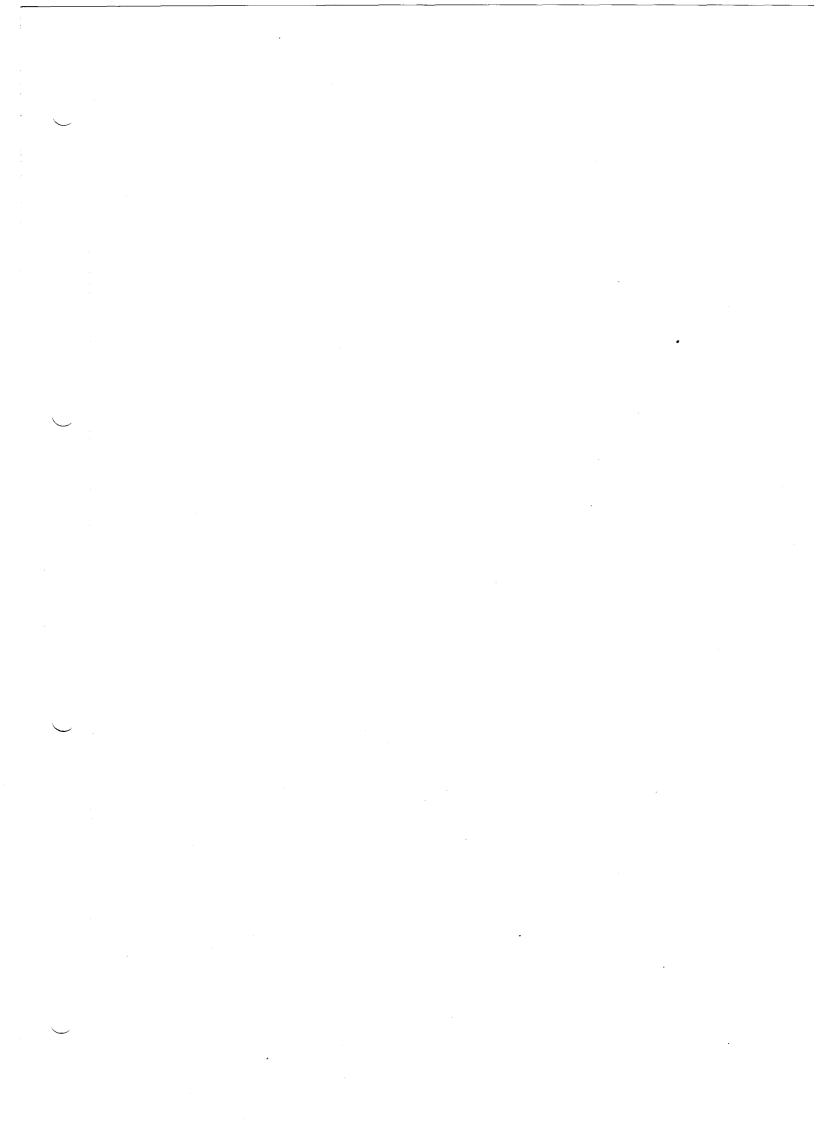


PART C OPERATING MODES

- C 1 Basic operating modes
 - RUN
 - PROG
 - MAN (Bit) - STEP
 - BREAK
 - DREAK
- C 1.1 Summary of operating modes
- C 1.2 Detailed description of operating modes
- C 2 Further operating modes (only for PCA2.M22/M32)

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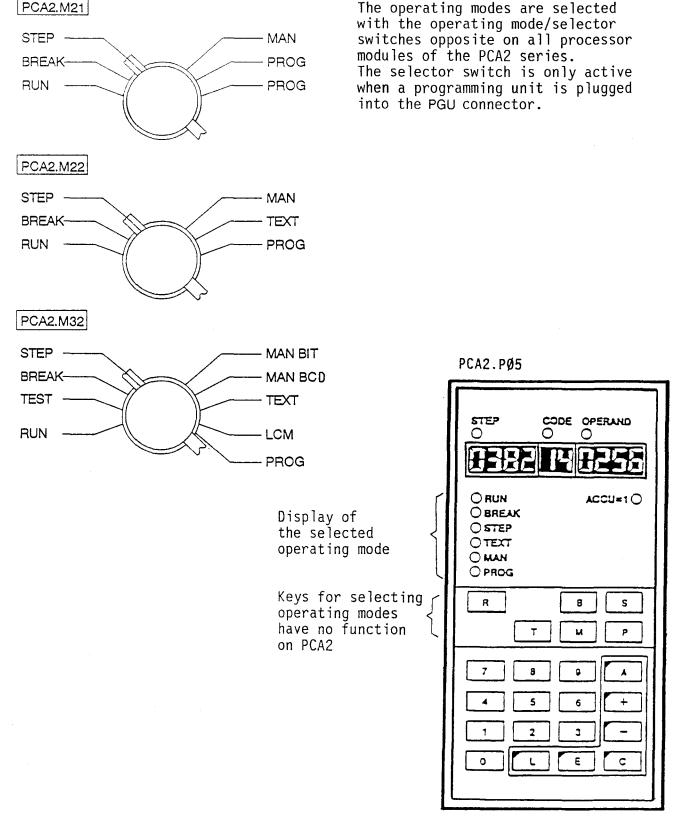
- C 2.1 TEST
- C 2.2 MAN or MAN BIT
- C 2.3 TEXT or text memory as data register
- C 2.4 MAN BCD
- C 2.5 LCM
- C 2.6 List of modules



General

In addition to the operating modes "programming" (PROG) and "normal program execution" (RUN), further useful operating modes are available for starting up and servicing. For this, only the compact programming unit PCA2.PØ5 is required for all SAIA[®]PLC.





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C 1 Basic operating modes

RUN Normal program processing

PROG A user program can be loaded into a RAM memory

- MAN Manual interrogation and setting of elements (inputs, outputs, flags, timers, counters)
- STEP Jump to a preselected step address (program line) of the user program and step-by-step operation
- BREAK Program processing up to a set "breakpoint" and subsequent step-by-step operation

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С	1.1	Summary	of	operating	modes

RUN	Normal program execution
	The PCA 2 is automatically in the RUN-mode when switching on if no programming unit is connected.
PROG	Programming
	A program can be stored in a RAM-memory (on the user socket of the PCA1) or overwritten (corrected).
	StepCodeOperandAxxxxxxxxx
	E x x x x x x x or C to delete a wrongly entered line
	+ Terminates the input.
	Test program +++ or
MAN *	* Manual testing or setting of elements
	(Elements = inputs, outputs, flags, counters, timers)
	Testing: $\begin{bmatrix} \text{Step} \\ x & x & x \\ y & y & y \\ y & y & y \\ y & y & y \\ y & y &$
	Element address
	Setting: $A \times x \times E 1$ so 0 or 0
STEP	+ Display showing where the program is.
	Jump to the preselected step address of the user program
	A 139 + → Program jumps to step 139, then + + + Step-by-step execution of the program with the result of the logic
	+ $+$ $+$ $+$ $+$ $+$ $+$ $+$ $+$ $+$
	In case of parallel programs, <u>only the activated parallel program</u> is executed in the STEP-mode.
BREAK	Interruption of the program run and subsequent step-by-step-operation
	+ Display showing where the program is.
	+ $+$ $+$ $+$ $+$ $+$ $+$ $+$ $+$ $+$
	In case of parallel programs, all programs are executed simultaneously (as in the RUN-mode).
	Setting of a breakpoint
	A 82∅ + → Program runs up to step 82∅, then
	+ [+ step-by-step operation skipping the "criterial" point.
If ACC follow	accumulator is used to indicate the result of the logic combinat C = 1 (conditions of the logic combination fulfilled = 1), the wing switching instructions are executed.
**) If the	e address of a timer or counter is preceded by a 3 (e.g. 326Ø for er 26Ø), t <u>he</u> value of this register can be read or entered manual

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RUN	if no progu	s auto rammin	matically g unit is	in the RUN-mode when switching on connected. itch must be in position RUN.
PROG	Programmin A program socket of	can be	stored in A2) or ove	n a RAM memory (on the user plug-in erwritten (corrected).
	A STEP	E	CODE xx	OPERAND xxxx
		E	xx	xxxx
		С	Deletes .	a wrongly entered line
		+	Terminat	es the input
		+	+ or [to display the program
MAN			STEP1)	<u>of elements</u> ts, flags, counters, timers) OPERAND
MAN	<u>Manual tes</u> (Elements = Testing:	ting o = inpu A		
MAN			STEP1)	OPERAND Ø/1 ───── display of the logic

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Continued from foo	otnote 1)				
Example: Input of	values 23419	or 127 i	nto coun	ters 29Ø c	or 291.
Input:	Display:	STEP	CODE	OPERAND	
A 329Ø		329Ø	ØY	ŶŶŶŶ	───Units ───Ten-thousands ───Always Ø
Input:	Display:	STEP	CODE	OPERAND	
A 329Ø E 23419 E 127		329Ø 329Ø 3291	ØY Ø2 Ø1	YYYY 3419 ØØ27	(wrong input)*
Correction before	storing				
C Ø 127*		3291 3291	ØØ ØØ*	ØØØØ Ø127	

* Values <10'000 have to be preceded by a leading 0.



STEP	+ Display showing where the program is.
	Jump to the preselected step address of the user program
	A 139 + Program jumps to step 139
	+ + step-by-step processing of the program with the linkage result being checkable: * ACCU = 1 2)
	Switching to RUN is always possible. In case of parallel program, <u>only the activated parallel</u> <u>program</u> is processed in the STEP mode.
BREAK	Interruption of the program run and subsequent step-by-step operation
	+ — — Display showing where the program is.
	+ + step-by-step execution of the program with the linkage result being checkable: ★ ACCU = 1 2>
	Switching to RUN is always possible. In case of parallel programs, <u>all programs</u> are processed simultaneously (as in the RUN-mode).
	Setting of a "breakpoint"
	A 820 + Program runs up to step 820 in slow RUN operation
	+ + step-by-step operation over the "critical" point.
	_
When LE	accumulator) is used to indicate the status of the logic combination D lights up, the ACCU = 1 (conditions of the logic combination fullfilled, linkage 1) , and the following switching instructions are executed.

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<u>C 2 Further operating modes (only for PCA2.M22 and M32)</u>
<u>C 2.1 "TEST" = checking of the ACCU state of the bit processor in the RUN-mode</u> (only PCA2.M32)
It is often of advantage to know the ACCU state of the bit processor at a certain program point in the RUN-mode.
Proceed as follows:
- Turn operating mode selector switch to position "TEST".
- Depress key [A], followed by the step address for checking the ACCU. Each key must be depressed (approx. Ø.5s) until the display has responded.
 In order to test the following step, + is despressed, for the preceding step - is depressed.
- The ACCU state is displayed in the CODE-field as follows:
CODE
If the display is effected in the left digit, the selected step address is in the program part of the word processor. If the display is effected in the <u>right</u> digit, the selected step address is in the program part of the <u>bit</u> processor.
. If the display remains out, the program does not execute the step address.
. Display \emptyset means ACCU = \emptyset
. Display 1 means ACCU = 1
. Display 2 means, that the ACCU-state rapidly oscillates between \emptyset and 1 (the display is updated every second).
Example: CODE [1] means that the ACCU = 1 and the selected address is in the bit program part.
<u>Remark:</u> Concerning the operating mode "TEST". The cycle time of the CPU in this operating mode is twice the cycle time in the operating mode "RUN", i.e. approx. 70µs instead of 35µs.

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C 2.2 "MAN" or "MAN BIT"

Manual access to the software date-time

Processor module M32 is only equipped with a software date-time which stops in case of voltage failure. The hardware date-time of this module is activated by using memory module PCA2.R27 on the upper main memory location and by inserting jumper "R27". Processor module M22 comes equipped with hardware date-time.

All programming units allow direct access to the software date-time (reading and writing).

The following table shows the signification and the numerical range for the addresses 4000...4007.

Address	Meaning	Numerical range
4ØØØ	Week of the year	153
4ØØ1	Day of the week	17
4ØØ2	Year (1989=89)	Ø99
4ØØ3	Month	112
4ØØ4	Day of the month (Feb = 28)*	131
4ØØ5	Hours	123
4ØØ6	Minutes	159
4ØØ7	Seconds	Ø59

*) Contrary to the hardware date-time R27, the software date-time does not take the leap years into account (February = 28 days).

You may enter a maximum of 2 digits which appear in the operand (see examples on the following page).



•	Examples	: Input	for	Thursday,	June	2nd,	89,	1Øh	12min	45s
---	----------	---------	-----	-----------	------	------	-----	-----	-------	-----

Input:	Display:	STEP	CODE	OPERAND
A 4000 E 22* E 4* E 89 E 6* E 2* E 10 E 12 E 45 +		4000 4000 4001 4002 4003 4004 4005 4006 4007	00 00 00 00 00 00 00	ØØYY ØØ22 ØØØ4 ØØ89 ØØØ6 ØØØ6 ØØ10 ØØ12 ØØ45

After entering the seconds (4007), key + is depressed, provided that the input corresponds to the actual time. Do not press key E again, since otherwise the input of the calendar week is erased.

• Display:

Input: Display:

A 4000 ++ ++ ++ ++ ++ ++ ++	4ØØØ 4ØØ1 4ØØ2 4ØØ3 4ØØ4 4ØØ5 4ØØ6 4ØØ7	00 00 00 00 00 00 00	ØØ22 ØØØ4 ØØØ6 ØØØ2 ØØ1Ø ØØ12 ØØ45	22nd week of the year Thursday 1989 June 2 1Øh 12min 45s 46s
				46s 47s



Input and reading of texts in the text memory

Input of texts is effected on RAM 6264 or 8464 or on the buffered RAM modules PCA1.R92/95/96 which are plugged onto the text socket.

The following 2 possibilities are available:

- a) Using one of the PCA programming units, connected via the PGU connector.
- b) With a peripheral unit with current loop interface, connected to the serial data interface.

For detailed description refer to manual Software level 2.

<u>Manual access to the text memory as data register (PAS 54 for M22 and M32, PAS 55 only for M32)</u>

In order to understand the monitor function of the system program, the formats which are used for organizing the various registers must be brought to mind:

Counter register	:	binary	16 bits
Text memory	:	binary	8 bits or 16 bits
(as data register)		or BCD	8 bits

For manual access to <u>the text memory as data register</u> the operating mode selector switch must be set to <u>"TEXT"</u>.

It is advantageous to use the data register for CPU M32 which is accessible in the operating mode "MAN BCD" or with PAS 56/57 (see chapter C 2.4).

- Display of the text memory contents
 - a) <u>Immediate display of a character value of 8 bits (1 byte) in binary</u> <u>notation</u>

Upon actuation of key [A], and subsequent input of the character number to be displayed (Ø...8191), the stored value (Ø...255) is displayed in the operand field in <u>binary notation</u>.

	(1 byte) in binary notation				
[-]		183Ø	ØØ	Ø157	

in the range	bit value (2 bytes) in bi Ø65'535 can be display	ed in the COD	E and OP	ERAND field.
Input:	Display:	STEP		OPERAND
		1831	E 3	4717
	Character no. selec- ted with key A]		
	Character for 2 byte	s		
	Value of the 2 chara 183Ø and 1831 (2 byt in binary notation			
	, the contents of transfe apacity of 16 bits.	rred counters	can be	displayed wi
c) Display of 1	character no. (1 byte = 8	bits) in BCD	-notatio	n
	key [C] (convert) a secon			
Input:	Display:	STEP	CODE	OPERAND
		1831	H Ø*	ØØ87
C		1001		
C -		1830	НØ	ØØ 9-
C -	Character no		H Ø	ØØ]9-]
C -	Character no Character for BCD-notation		ĤØ	ØØ 9-
C -	Character for		Ĥ Ø	ØØ 9-
C -	Character for BCD-notation	183Ø	ĤØ	ØØ]9-
C -	Character for BCD-notation Always Ø ØØ 1 byte in BCD	183Ø	Ĥ Ø	ØØ 9-



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Real BCD-bit patterns are displayed as decimals. If other characters are present as e.g. at character no. $183\emptyset$, these are no BCD-bit patterns. In order to be able to interpret their values nevertheless, the following 7-segment characters are defined in the OPERAND:

Binary value	7-segment P1Ø	character PØ5
1Ø		
11		E
12		8
13		E
14		2
15	blank	blank

• <u>Manual data inputs into the text memory</u> (limited RAM-memory in this area)

Key [A] : subsequent input of the character no., at which the value is to be stored

Key [E] : clears the old value and permits new input

Key C : <u>before</u> key E means "convert" <u>after</u> key E means "clear"

Key [+], [-], [A], [E]: cause storage of the value introduced

Corresponding to the reading of data, 3 cases are distinguished for the manual input of data:

a) <u>Input of a binary value of 1 byte (e.g. 48) at a character no.</u> (e.g. 7436)

Input:		Display:	STEP	CODE	OPERAND
Α	7436		7436	ØØ	ØXXX
E	48		7436	ØØ	ØØ48
+			7437	ØØ	ØYYY

Input:	Display:	STEP	CODE	OPERAND
A 7457	1)	7457	ØØ	ØXXX
С	2)	7457	EY*	YYYY
E 1487	3)	7457	E1*	Ø487
C Ø1487	,	7457	EØ*	1487
+		7459 4)	EZ*	ZZZZ
	ne higher address of re [E] results in the		-	
3) If values	s < 10'000 are entere on with [C].			
4) The chara	icter no. is automati	cally increase	ed by 2	•
-		-	·	
) Input of a E	acter no. is automati 3CD-value (e.g. 3Ø) a from Ø99 ≙ 1 byte	t character n	o. 766Ø	
) Input of a E	BCD-value (e.g. 3Ø) a	t character n	o. 766Ø	
) <u>Input of a B</u> only values	<u>3CD-value (e.g. 3Ø) a</u> from Ø99 ≙ 1 byte	t character n can be enter	o. 766Ø ed)	(in BCD-notat
) <u>Input of a E</u> only values Input:	<u>3CD-value (e.g. 3Ø) a</u> from Ø99 ≙ 1 byte	<u>t character n</u> can be enter STEP	<u>o. 766Ø</u> ed) CODE	<u>(in BCD-notat</u>
) <u>Input of a E</u> only values Input: A 766Ø	<u>3CD-value (e.g. 3Ø) a</u> from Ø99 ≙ 1 byte	t character no can be enter STEP 766Ø	o. 766Ø ed) CODE ØØ	(in BCD-notat OPERAND ØXXX
) <u>Input of a E</u> only values Input: A 766Ø C	<u>3CD-value (e.g. 3Ø) a</u> from Ø99 ≙ 1 byte	t character no can be enter STEP 766Ø 766Ø	o. 766Ø ed) CODE ØØ EY*	(in BCD-notat OPERAND ØXXX YYYY
) <u>Input of a E</u> only values Input: A 766Ø C C	<u>3CD-value (e.g. 3Ø) a</u> from Ø99 ≙ 1 byte	t character no can be enter STEP 766Ø 766Ø 766Ø	o. 766Ø ed) CODE ØØ EY* HØ*	(in BCD-notat OPERAND ØXXX YYYY ØØZZ
) <u>Input of a E</u> only values Input: A 766Ø C C E 3Ø	<u>3CD-value (e.g. 3Ø) a</u> from Ø99 ≙ 1 byte	t character no can be enter STEP 766Ø 766Ø 766Ø 766Ø	<u>o. 766Ø</u> ed) CODE ØØ EY* HØ* HØ*	(in BCD-notat OPERAND ØXXX YYYY ØØZZ ØØ3Ø
) <u>Input of a E</u> only values Input: A 766Ø C C E 3Ø	<u>3CD-value (e.g. 3Ø) a</u> from Ø99 ≙ 1 byte	t character no can be enter STEP 766Ø 766Ø 766Ø 766Ø	<u>o. 766Ø</u> ed) CODE ØØ EY* HØ* HØ*	(in BCD-notat OPERAND ØXXX YYYY ØØZZ ØØ3Ø

*) Characters apply to PCA2.PØ5.

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Manually reading out and entering BCD-values into the word register Display of a stored value By depressing key $[A]$ which is followed by the word address Rn (\emptyset 999) the value is displayed in the operand (2 digits). Input of a value into the word register . Key $[A]$ followed by the word address (\emptyset 999). . Key $[E]$ clears the display and allows a new input. . The value is keyed in and terminated with \pm , $[-]$, $[A]$, $[E]$ Examples: - The BCD-value 35 is to be entered at word address 51 \emptyset : $[A]$ 51 \emptyset $[E]$ 35 \pm - The BCD-value 68 is to be entered at word address 174: $[A]$ 174 $[E]$ 65 $[C]$ 68 \pm The value can be corrected with key "clear" - The BCD-value 126'537 are entered at the word addresses 622, 623 and 624: [A] 622 $[E]$ 12 [A] 622 $[E]$ 12 When reading the whole register block, check whether a \emptyset is at the addresses 629 and 621. Otherwise, \emptyset must be entered. - The negative BCD-value -126'537 is to be entered using the register block R624: Proceed as above, with the difference that a 9 is to be entered for the uper value of R62 \emptyset which is evaluated as negative character by the processor. $[A]$ 62 \emptyset $[E]$ 9 \emptyset (621) $[E]$ 9 \emptyset (621) $[E]$ 9 \emptyset (622) $[E]$ 12	<u>C 2.4 "MAN BCD" = manual access to the word register as well as to the data</u>
Display of a stored value By depressing key \bigcirc which is followed by the word address Rn (Ø999) the value is displayed in the operand (2 digits). Input of a value into the word register . Key \bigcirc followed by the word address (Ø999). . Key \bigcirc clears the display and allows a new input. The value is keyed in and terminated with $+, _, \bigcirc$ \bigcirc \bigcirc clears the display and allows a new input. The value is keyed in and terminated with $+, _, \bigcirc$ \bigcirc \bigcirc clears the display and allows a new input. The value is keyed in and terminated with $+, _, \bigcirc$ \bigcirc \bigcirc clears to be entered at word address 510: \bigcirc The BCD-value 35 is to be entered at word address 174: \bigcirc 174 \bigcirc 65 \bigcirc 68 $+$ The value can be corrected with key "clear" - The BCD-value 126'537 are entered at the word addresses 622, 623 and 624: \bigcirc 622 \bigcirc 12 \bigcirc 65 \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc	register of the user memory (only for PCA2.M32)
By depressing key A which is followed by the word address Rn (Ø999) the value is displayed in the operand (2 digits). Input of a value into the word register . Key A followed by the word address (Ø999). . Key E clears the display and allows a new input. . The value is keyed in and terminated with +, -, A, E Examples: - The BCD-value 35 is to be entered at word address 51Ø: A 51Ø E 35 + - The BCD-value 68 is to be entered at word address 174: A 174 E 65 C 68 + The value can be corrected with key "clear" - The BCD-value 126'537 are entered at the word addresses 622, 623 and 624: A 622 E 12 (623) E 65 (624) E 37 + When reading the whole register block, check whether a Ø is at the addresses 62Ø and 621. Otherwise, Ø must be entered. - The negative BCD-value -126'537 is to be entered using the register block R624: Proceed as above, with the difference that a 9 is to be entered for the upper value of R62Ø which is evaluated as negative which is evaluated as negative which is evaluated as negative A 62Ø E 9Ø (621) E Ø (622) E 12	
value is displayed in the operand (2 digits). Input of a value into the word register . Key A followed by the word address (Ø999). . Key E clears the display and allows a new input. . The value is keyed in and terminated with $+, -, A$, E Examples: - The BCD-value 35 is to be entered at word address 510: A 510 E 35 $+$ - The BCD-value 68 is to be entered at word address 174: A 174 E 65 C 68 $+$ The value can be corrected with key "clear" - The BCD-value 126'537 are entered at the word addresses 622, 623 and 624: A 622 E 12 (623) E 65 (624) E 37 $+$ When reading the whole register block, check whether a Ø is at the addresses 62Ø and 621. Otherwise, Ø must be entered. - The negative BCD-value -126'537 is to be entered using the register block R624 Proceed as above, with the difference that a 9 is to be entered for the upper value of R62Ø which is evaluated as negative character by the processor. A 62Ø E 9Ø (621) E Ø (622) E 12	Display of a stored value
 Key A followed by the word address (Ø999). Key E clears the display and allows a new input. The value is keyed in and terminated with +, -, A, E Examples: The BCD-value 35 is to be entered at word address 51Ø: A 51Ø E 35 + The BCD-value 68 is to be entered at word address 174: A 174 E 65 C 68 + The value can be corrected with key "clear" The BCD-value 126'537 are entered at the word addresses 622, 623 and 624: A 622 E 12 (623) E 65 (624) E 37 + When reading the whole register block, check whether a Ø is at the addresses 62Ø and 621. Otherwise, Ø must be entered. The negative BCD-value -126'537 is to be entered using the register block R624: The negative BCD-value -126'537 is to be entered using the register block R620 Proceed as above, with the difference that a 9 is to be entered of the upper value of R62Ø must be entered. A 62Ø E 9Ø (621) E Ø (622) E 12 	
 Key [E] clears the display and allows a new input. The value is keyed in and terminated with +, -, A, E Examples: The BCD-value 35 is to be entered at word address 510: A 510 E 35 + The BCD-value 68 is to be entered at word address 174: A 174 E 65 C 68 + The value can be corrected with key "clear" The BCD-value 126'537 are entered at the word addresses 622, 623 and 624: A 622 E 12 (623) E 65 (624) E 37 + When reading the whole register block, check whether a Ø is at the addresses 62Ø and 621. Otherwise, Ø must be entered. The negative BCD-value -126'537 is to be entered using the register block R624: Proceed as above, with the difference that a 9 is to be entered using the register block R624: Proceed as above, with the difference that a 9 is to be entered using the register block R624: A 62Ø E 9Ø (621) E Ø (622) E 12 	Input of a value into the word register
 The BCD-value 35 is to be entered at word address 510: A 510 E 35 + The BCD-value 68 is to be entered at word address 174: A 174 E 65 C 68 + The value can be corrected with key "clear" The BCD-value 126'537 are entered at the word addresses 622, 623 and 624: A 622 E 12 (623) E 65 (624) E 37 + When reading the whole register block, check whether a Ø is at the addresses 620 and 621. Otherwise, Ø must be entered. The negative BCD-value -126'537 is to be entered using the register block R624: Proceed as above, with the difference that a 9 is to be entered using the register block R624: A 620 E 90 (621) E Ø (622) E 12 	. Key [E] clears the display and allows a new input.
 A 51Ø E 35 + The BCD-value 68 is to be entered at word address 174: A 174 E 65 C 68 + The value can be corrected with key "Clear" The BCD-value 126'537 are entered at the word addresses 622, 623 and 624: A 622 E 12 (623) E 65 (624) E 37 + When reading the whole register block, check whether a Ø is at the addresses 62Ø and 621. Otherwise, Ø must be entered. The negative BCD-value -126'537 is to be entered using the register block R624: Proceed as above, with the difference that a 9 is to be entered for the upper value of R62Ø which is evaluated as negative character by the processor. A 62Ø E 9Ø (621) E Ø (622) E 12 	Examples:
- The BCD-value 68 is to be entered at word address 174: A 174 E 65 C 68 \div The value can be corrected with key "clear" - The BCD-value 126'537 are entered at the word addresses 622, 623 and 624: A 622 E 12 (623) E 65 (624) E 37 \div When reading the whole register block, check whether a Ø is at the addresses 62Ø and 621. Otherwise, Ø must be entered. - The <u>negative</u> BCD-value -126'537 is to be entered using the register block R624: Proceed as above, with the difference that a 9 is to be entered for the upper value of R62Ø which is evaluated as <u>negative</u> character by the processor. A 62Ø E 9Ø (621) E Ø (622) E 12	- The BCD-value 35 is to be entered at word address 510:
A174E65C68+The value can be corrected with key "clear"The value can be corrected with key "clear"The BCD-value 126'537 are entered at the word addresses 622, 623 and 624:A622E12 $3 - 7$ R624 R623 R624Value R624(623)E65 $9 - 0$ R622 R621Value R629(624)E37+ $9 - 0$ Value R629When reading the whole register block, check whether a Ø is at the addresses 62Ø and 621. Otherwise, Ø must be entered.12'65'37For megative BCD-value -126'537 is to be entered using the register block R624:Proceed as above, with the difference that a 9 is to be entered for the upper value of R62Ø which is evaluated as negative character by the processor. $3 - 7 - 12'65'37$ R620 $9 - 0$ R624 R621 R620 $R620$ $R620$ Value R621 R620 $R620$ A62ØE9Ø (621)E90R621 R620 R62012'65'37	A 51Ø E 35 +
The value can be corrected with key "clear" - The BCD-value 126'537 are entered at the word addresses 622, 623 and 624: $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	- The BCD-value 68 is to be entered at word address 174:
key "clear" - The BCD-value 126'537 are entered at the word addresses 622, 623 and 624: $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	A 174 E 65 C 68 +
 The BCD-value 126'537 are entered at the word addresses 622, 623 and 624: A 622 E 12 (623) E 65 (624) E 37 + When reading the whole register block, check whether a Ø is at the addresses 62Ø and 621. Otherwise, Ø must be entered. The negative BCD-value -126'537 is to be entered using the register block R624: Proceed as above, with the difference that a 9 is to be entered using the register block R620 year of the upper value of R620 y	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	- The BCD-value 126'537 are entered at the word addresses 622, 623
(623) E 65 (624) E 37 + $R622$ $R621$ 0 0 $R620$ $R620When reading the whole register block, check whether a 0 is at theaddresses 620 and 621. Otherwise, 0 must be entered.- The negative BCD-value -126'537 is to be entered using the register blockR624:Proceed as above, with thedifference that a 9 is to beentered for the upper value of R620which is evaluated as negativecharacter by the processor.A 620 E 90(621) E 0(622) E 12$	A 622 E 12 3 7 R624
(624) E 37 + $0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 $	
addresses 620 and 621 . Otherwise, 0 must be entered. - The negative BCD-value -126'537 is to be entered using the register block R624: Proceed as above, with the difference that a 9 is to be entered for the upper value of R620 which is evaluated as negative character by the processor. A 620 E 90 (621) E 0 (622) E 12	
R624: Proceed as above, with the difference that a 9 is to be entered for the upper value of R62Ø which is evaluated as <u>negative</u> character by the processor. $A 62\emptyset E 9\emptyset$ (621) $E \emptyset$ (622) $E 12$	
difference that a 9 is to be entered for the upper value of R620 which is evaluated as negative character by the processor. A 620 E 90 (621) E 0 (622) E 12 655 R623 Value R620 R621 9 0 R620 (622) E 12	- The <u>negative</u> BCD-value -126'537 is to be entered using the register block R624:
(621) E Ø (622) E 12	difference that a 9 is to be65R623Valueentered for the upper value of R62Ø12R622-12'65'37which is evaluated as negativeØØR621-
(622) E 12	A 62Ø E 9Ø
	(621) E Ø
	(622) E 12
etc.	etc.

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SAIA[®]PLC Programmable controllers

- A binary value is to be entered at word address 715:

- 1100 0010 B (binary)
- ≙ C 2 H (hexa)

≙ 194 D (decimal)

[A] 715

C E 194 +

Key "C" (convert) causes conversion from BCD ---> binary of the value subsequently entered in BCD-representation. An acknowledgement is effected in the OPERAND by the character \models 194.

Note:

- Every input is terminated with [+], [-] or [A].
- The above example shows that C before E results in the conversion of the input from BCD ---> binary or from binary ---> BCD. BCD-format is always selected by depressing [A].

Manually reading out and entering values into the data register of the user memory

The user memory of the M32 has a data memory of 8K times 8 bits, which can be accessed in the user program via the instructions PAS 56 and PAS 57. In order to be able to understand the supervisory function of the system program recall the representation of the various registers.

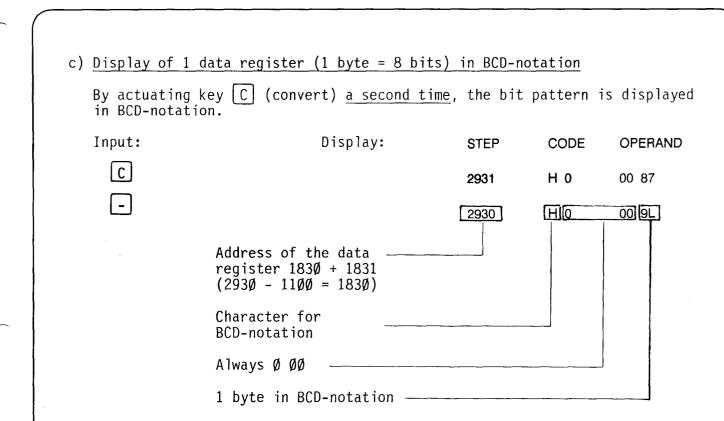
Counter register: binary 16 bits Word register : BCD 8 bits or 5 x 8 bits Text memory : binary 8 bits or 16 bits or BCD 8 bits

The word register and data register can be manually accessed in the operating mode "MAN BCD". In order to avoid conflicts with the 1023 word registers, the value 1100 must be added to the data addresses 0...8191 entered.

	a value of 8 bits ts of data register				
By actuati the stored operand fi	ng key A and sub value (Ø255) i eld.	sequently e s displayed	ntering a l in binar	address 29 Ty represe	931 (1831 + 11ØØ), entation in the
Input:	ł	Display:	STEP	CODE	OPERAND
A 293	1		2931	ØØ	Ø135
	Address of the d registers 1831 (2931 - 1100 = 18				
	Always ØØ Ø ———]
	Value of 8 bits in binary repres				
-			293Ø	ØØ	Ø157
	the contents of O				•
notation Actuating selected c to form a	the contents of 2 the key [C] (conver ata register, the 16 bit-value (2 by 5'535 can be displa	rt) <u>once</u> ha value of th tes) in bin	ters (2 b s the res e precedi ary notat	oyte = 16 sult that ng regist tion. As a	bits) in binary in addition to th ter can be combine a result, values
notation Actuating selected c to form a	the key [C] (conver ata register, the 16 bit-value (2 by 5'535 can be displa	rt) <u>once</u> ha value of th tes) in bin	ters (2 b s the res e precedi ary notat	oyte = 16 sult that ng regist tion. As a	bits) in binary in addition to th ter can be combine a result, values
notation Actuating selected of to form a from Ø6	the key [C] (conver ata register, the 16 bit-value (2 by 5'535 can be displa	rt) <u>once</u> ha value of th tes) in bin ayed in the	ters (2 b s the res e precedi ary notat CODE and	oyte = 16 sult that ng regist tion. As a l OPERAND	bits) in binary in addition to th ter can be combine a result, values field.
notation Actuating selected of to form a from Ø6 Input:	the key [C] (conver ata register, the 16 bit-value (2 by 5'535 can be displa	rt) <u>once</u> ha value of th tes) in bin ayed in the Display: dress 1831 y A	ters (2 b s the res e precedi ary notat CODE and STEP	oyte = 16 ault that ng regist ion. As a OPERAND CODE	bits) in binary in addition to th ter can be combine a result, values field. OPERAND
notation Actuating selected of to form a from Ø6 Input:	the key [C] (conver ata register, the 16 bit-value (2 by 5'535 can be displa Data register ado selected with key	rt) <u>once</u> ha value of th tes) in bin ayed in the Display: dress 1831 y A 831)	ters (2 b s the res e precedi ary notat CODE and STEP	oyte = 16 ault that ng regist ion. As a OPERAND CODE	bits) in binary in addition to th ter can be combine a result, values field. OPERAND
notation Actuating selected of to form a from Ø6 Input:	the key [C] (conver ata register, the 16 bit-value (2 by 5'535 can be displa Data register add selected with key (2931 - 1100 = 18	rt) <u>once</u> ha value of th tes) in bin ayed in the Display: dress 1831 y A 331) bytes egisters 	ters (2 b s the res e precedi ary notat CODE and STEP	oyte = 16 ault that ng regist ion. As a OPERAND CODE	bits) in binary in addition to th ter can be combine a result, values field. OPERAND
notation Actuating selected of to form a from Ø6 Input: C In this wa	the key [C] (conver ata register, the 16 bit-value (2 by 5'535 can be displa Data register add selected with key (2931 - 1100 = 12 Character for 2 b Value of the 2 re 1830 and 1831 (2	rt) <u>once</u> ha value of th tes) in bin ayed in the Display: dress 1831 y A B31) bytes bytes bytes) on transferre	ters (2 b s the res e precedi ary notat CODE and STEP	oyte = 16 sult that ng regist ion. As a OPERAND CODE	<u>bits) in binary</u> in addition to th ter can be combine a result, values field. OPERAND 4717
notation Actuating selected of to form a from Ø6 Input: C In this wa	the key [C] (conver ata register, the 16 bit-value (2 by 5'535 can be displa Data register add selected with key (2931 - 1100 = 18 Character for 2 b Value of the 2 ro 1830 and 1831 (2 in binary notations)	rt) <u>once</u> ha value of th tes) in bin ayed in the Display: dress 1831 y A B31) bytes bytes bytes) on transferre	ters (2 b s the res e precedi ary notat CODE and STEP	oyte = 16 sult that ng regist ion. As a OPERAND CODE	<u>bits) in binary</u> in addition to th ter can be combine a result, values field. OPERAND 4717

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16C



Real BCD-bit patterns are displayed as decimals. If other characters are present as e.g. in the data register $183\emptyset$, these are no BCD-bit patterns. In order to be able to interpret their values nevertheless, the following 7-segment characters have been defined:

Binary	Charact	
value	P1Ø	PØ5
1Ø		
11		E
12		
13		
14	E	B
15	blank	blank

The characters of the P05 are used in the explanations.

17C

Manually entering data into the (RAM-memory is required in this area)	ne <u>data reg</u> i	<u>ster</u>		
Key A : Subsequently enter t value is to be store				
Key [E] : Clears the old value	e and permit	s new input		
	s "convert" s "clear"			
Keys +, -, A, E : cause s	storage of t	he value in	itroduced	
As with reading of data, <u>3 cas</u> manually.	<u>ses</u> can be d	istinguishe	ed when e	ntering data
1) <u>Input of a binary value of</u> (e.g. register 6336, addr.	<u>1 byte</u> (e.g = 6336 + 11	48) into a ØØ = 7436)	a data re	gister
Input:	Display:	STEP	CODE	OPERAND
A 7436		7436	ØØ	ØXXX
E 48		7436	ØØ	ØØ48
+		7437	ØØ	ØYYY
2) <u>Input of a binary value of</u> 6356 and 6357 (addr. = reg.	<u>2 bytes</u> (e. + 1100)	g. 1487) ir	nto the d	ata registers
^ Input:	Display:	STEP	CODE	OPERAND
A 7457 1)		7457	ØØ	ØXXX
() 2)		7457	ΕΥ *	YYYY
E 1487 3)		7457	E1 *	Ø487
C Ø1487		7457	EØ *	1487
+		7459 4)	EZ *	ZZZZ
1) Always the higher addres	ss of a pair	of 2 bytes	s is ente	red.
²) C before E causes co	onversion to	2 bytes.		
з) If values < 10'ØØØ are e Correct with [С].	entered, a Ø	must be er	ntered fi	rst.
✤) The data register addres	s is automa	tically inc	reased b	y 2.
*) For PCA2.PØ5				

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3) Input of a BCD-value (e.g. 3Ø) into data register 6560 (in BCDnotation only values from $\emptyset \dots 99 \cong 1$ byte can be entered).

Input:	Display:	STEP	CODE	OPERAND
A 766Ø (656Ø + 11ØØ)		766Ø	ØØ	ØXXX
C		766Ø	EY *	YYYY
C		766Ø	HØ *	ØØZZ
E 3Ø		766Ø	HØ *	ØØ3Ø
+		7661	HØ *	ØØAB

*) For PCA2.PØ5

C 2.5 "LCM" = Load Copy Memory (only PCA2.M32)

- Virtually all memory modules can be used with PCA2.M32. The full capacity, however, is obtained only by using the modules R26 and R27.
- Copying is effected from the upper plug-in location of the CPU (main memory location) to the lower plug-in location (copy memory location). It is not important, whether programs or texts are copied. After transferring a program word, the contents are compared. If the contents of master and copy differ, the process will be stopped at once and the error address will be displayed.
- Two programs on two modules (RAM or EPROM) can be compared to each other in a similar way.

Examples:

. Input for copying

1200 (start address) E ØØ 3800 (end address) |L| "Load"

. Input for comparing the contents

[A	12ØØ (sta	rt address)	E) ØØ	38ØØ	(end	address)	C	COMPARE
-----	-----------	-------------	---	------	------	------	----------	---	---------

- Copying is effected at different speeds depending on the memory to be loaded:

- . For loading into RAM (from RAM or EPROM) copying takes approx. 1s/1K.
- . For loading into $\overline{\text{EPROM}}$ (from RAM or EPROM) copying takes approx. 100/100 s/1K.

The CPU is able to choose the right speed itself by means of self-testing.

If a certain text area is to be copied, the text numbers must be converted to step addresses as follows:

Starting text no. $x5 \cong$ starting step address Destination text no. $x5 (+4) \cong$ destination step address

Example:

Starting text no.150 \triangleq starting step address750Destination text no.200 \triangleq destination step address1004

Note: Use power supply module PCA2.N3Ø/31 and disconnect the I/O cards from the bus connectors for copying into EPROM.

20C

<u>C 2.6</u> List of modules

21C

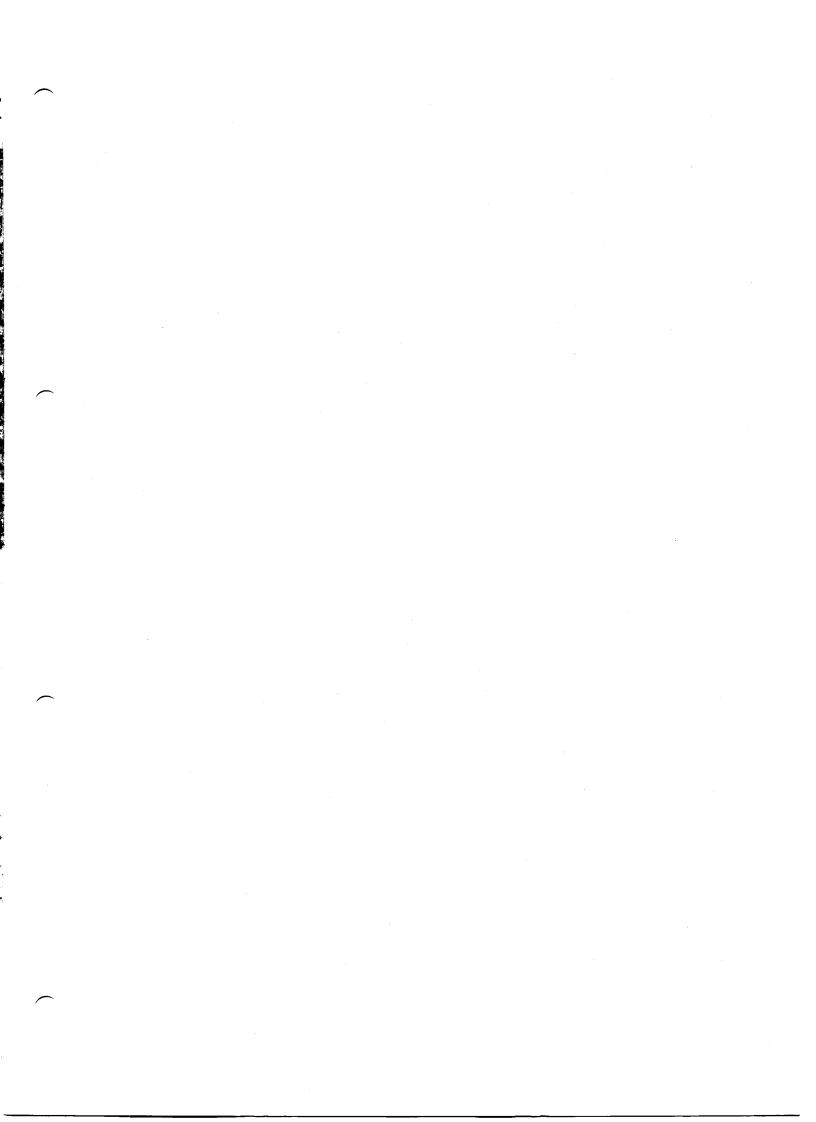
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Notes:				
	· .			
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